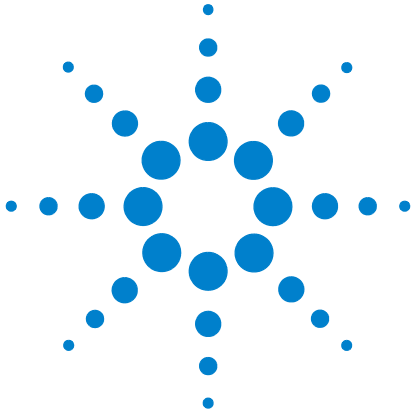

Agilent U7238A MIPI D-PHY Conformance Test Application

Methods of Implementation

Agilent Technologies

Notices

Manual Part Number

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Agilent Technologies, Inc.
1900 Garden of the Gods Road
Colorado Springs, CO 80907 USA

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A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

MIPI D-PHY Conformance Test Application — At A Glance

The Agilent U7238A MIPI D-PHY Conformance Test Application is developed to cater the Electrical Characteristics tests, Global Operations tests and HS Data-Clock tests.

The MIPI D-PHY automated test application allows the testing of all MIPI devices with the Agilent 80000, 90000, or 9000 Series Infiniium oscilloscope based on the *MIPI Alliance Standard for D-PHY v0.9* specification. MIPI stands for Mobile Industry Processor Interface. The MIPI alliance is a collaboration of mobile industry leader with the objective to define and promote open standards for interfaces to mobile application processors.

The MIPI D-PHY Conformance Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Allows you to determine the number of trials for each test, with the new multi trial run capability.
- Provides detailed information of each test that has been run. The result of maximum twenty five worst trials can be displayed at any one time.
- Creates a printable HTML report of the tests that have been run.

Required Equipment and Software

In order to run the MIPI D-PHY automated tests, you need the following equipment and software:

- 80000, 90000, or 9000 Series Infiniium oscilloscope. Agilent recommends using 4 GHz and higher bandwidth oscilloscope.
- Version 2.01 or greater of the Infiniium software (90000 Series and 9000 Series).
- Version 5.71 or greater of the Infiniium software (80000 Series).
- U7238A MIPI D-PHY Conformance Test Application, version 1.2 or higher.
- Differential probe amplifier, with the minimum bandwidth of 5 GHz.
- E2677A differential solder-in probe head, E2675A differential browser probe head, E2678A differential socket probe head and E2669A differential kit which includes E2675A, E2677A and E2678A are recommended.
- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).

- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).

Below are the required licenses:

- U7238A MIPI D-PHY Conformance Test Application license.
- N5414A InfiniiScan software license.

In This Book

This manual describes the tests that are performed by the MIPI D-PHY Conformance Test Application in detail.

- Chapter 1, "Installing the MIPI D-PHY Conformance Test Application" shows how to install and license the automated test application software (if it was purchased separately).
- Chapter 2, "Preparing to Take Measurements" shows how to start the MIPI D-PHY Conformance Test Application and gives a brief overview of how it is used.
- Part I, "Electrical Characteristics" contains 3 chapters (Chapter 3 - Chapter 5), emphasizing on HS Data, HS Clock and LP Transmitter tests.
- Chapter 3, "High Speed Data Transmitter (HS Data Tx) Electrical Tests" describes the high speed data transmitter tests including V_{CMTX}, $\Delta V_{CMTX(1,0)}$, V_{OD}, ΔV_{OD}, V_{OHHS}, $\Delta V_{CMTX(HF)}$, $\Delta V_{CMTX(LF)}$, t_R and t_F tests.
- Chapter Part I, "High Speed Clock Transmitter (HS Clock Tx) Electrical Tests" describes the high speed clock transmitter tests including V_{CMTX}, $\Delta V_{CMTX(1,0)}$, V_{OD}, ΔV_{OD}, V_{OHHS}, $\Delta V_{CMTX(HF)}$, $\Delta V_{CMTX(LF)}$, t_R and t_F tests.
- Chapter 4, "Low Power Transmitter (LP Tx) Electrical Tests" shows how to run the low power transmitter tests including V_{OH}, V_{OL}, T_{RLP}, T_{FLP}, T_{REOT}, $T_{LP\text{-}PULSE\text{-}TX}$, $T_{LP\text{-}PER\text{-}TX}$ and C_{LOAD} tests.
- Part II, "Global Operation" contains 2 chapters (Chapter 6 - 7) which covers Data and Clock Transmitter tests.
- Chapter 6, "Data Transmitter (Data Tx) Global Operation Tests" shows how to run the data transmitter tests including Data T_{LPX}, $T_{HS\text{-}PREPARE}$, $T_{HS\text{-}PREPARE} + T_{HS\text{-}ZERO}$, $T_{HS\text{-}TRAIL}$, T_{EOT} and $T_{HS\text{-}EXIT}$ tests.
- Chapter 7, "Clock Transmitter (Clock Tx) Global Operation Tests" shows how to run the clock transmitter tests including Clock $T_{HS\text{-}EXIT}$, Clock T_{LPX}, $T_{CLK\text{-}PREPARE}$, $T_{CLK\text{-}PREPARE} + T_{CLK\text{-}ZERO}$, $T_{CLK\text{-}PRE}$, $T_{CLK\text{-}TRAIL}$ and T_{EOT} tests.
- Part III, "HS Data-Clock Timing" contains 1 chapter (Chapter 8) which covers HS Clock Instantaneous, HS Clock Rising Edge Alignment to First Payload Bit and Data-to-Clock Skew tests.
- Chapter 8, "High Speed (HS) Data-Clock Timing Tests" shows how to run the HS Clock Instantaneous, HS Clock Rising Edge Alignment to First Payload Bit and Data-to-Clock Skew tests.
- Part IV, "Appendices" contains calibration and probing information.
- Chapter 9, "Calibrating the Infiniium Oscilloscopes and Probes" describes how to calibrate the oscilloscope in preparation for running the MIPI D-PHY automated tests.
- Chapter 10, "InfiniiMax Probing" describes the probe amplifier and probe head recommendations for MIPI D-PHY conformance testing.

See Also

- The MIPI D-PHY Conformance Test Application's online help, which describes:
  - Starting the MIPI D-PHY conformance test application.
  - Creating or opening a test project.
  - Setting up MIPI D-PHY test environment.
  - Selecting tests.
  - Configuring selected tests.
  - Connecting the oscilloscope to the DUT.
  - Running tests.
  - Viewing test results.
  - Viewing/printing the HTML test report.
  - Understanding the HTML report.
  - Saving test projects.

Contact Agilent

For more information on MIPI D-PHY Conformance Test Application or other Agilent Technologies' products, applications and services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Phone or Fax

United States:

(tel) 800 829 4444

(fax) 800 829 4433

Canada:

(tel) 877 894 4414

(fax) 800 746 4866

China:

(tel) 800 810 0189

(fax) 800 820 2816

Europe:

(tel) 31 20 547 2111

Japan:

(tel) (81) 426 56 7832

(fax) (81) 426 56 7840

Korea:

(tel) (080) 769 0800

(fax) (080) 769 0900

Latin America:

(tel) (305) 269 7500

Taiwan:

(tel) 0800 047 866

(fax) 0800 286 331

Other Asia Pacific Countries:

(tel) (65) 6375 8100

(fax) (65) 6755 0042

E-mail: tm_ap@agilent.com

Contents

3 High Speed Data Transmitter (HS Data Tx) Electrical Tests

1 Installing the MIPI D-PHY Conformance Test Application

If you purchased the U7238A MIPI D-PHY Conformance Test Application separately, you need to install the software and license key.

Installing the Software

1 Make sure you have version 2.01 or greater of the baseline software (90000 Series or 9000 Series Infiniium oscilloscope) OR version 5.71 or greater of the Infiniium software (80000 Series Infiniium oscilloscope), by choosing **Help>About Infiniium...** from the main menu.

2 To obtain the MIPI D-PHY Conformance Test Application, go to Agilent website: http://www.agilent.com/find/U7238A.

3 The link for MIPI D-PHY Conformance Test Application will appear. Double-click on it and follow the instructions to download and install the application software.

Installing the License Key

1 Request a license code from Agilent by following the instructions on the Entitlement Certificate.

You will need the oscilloscope's "Option ID Number", which you can find in the **Help>About Infiniium...** dialog box.

2 After you receive your license code from Agilent, choose **Utilities>Install Option License...**.

3 In the Install Option License dialog, enter your license code and click **Install License**.

4 Click **OK** in the dialog that tells you to restart the Infiniium oscilloscope application software to complete the license installation.

5 Click **Close** to close the Install Option License dialog.

6 Choose **File>Exit**.

7 Restart the Infiniium oscilloscope application software to complete the license installation.

2 Preparing to Take Measurements

Before running the MIPI D-PHY automated tests, you should calibrate the oscilloscope and probe. No test fixture is required for this MIPI D-PHY application. After the oscilloscope and probe have been calibrated, you are ready to start the MIPI D-PHY Conformance Test Application and perform the measurements.

Calibrating the Oscilloscope

If you haven't already calibrated the oscilloscope and probe, see Chapter 9, "Calibrating the Infiniium Oscilloscopes and Probes".

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

NOTE If you switch cables between the channels or other oscilloscopes, it is necessary to perform cable and probe calibration again. Agilent recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the MIPI D-PHY Conformance Test Application

1 To start the MIPI D-PHY Conformance Test Application: From the Infiniium oscilloscope's main menu, choose **Analyze>Automated Test Apps>MIPI D-PHY Test**.

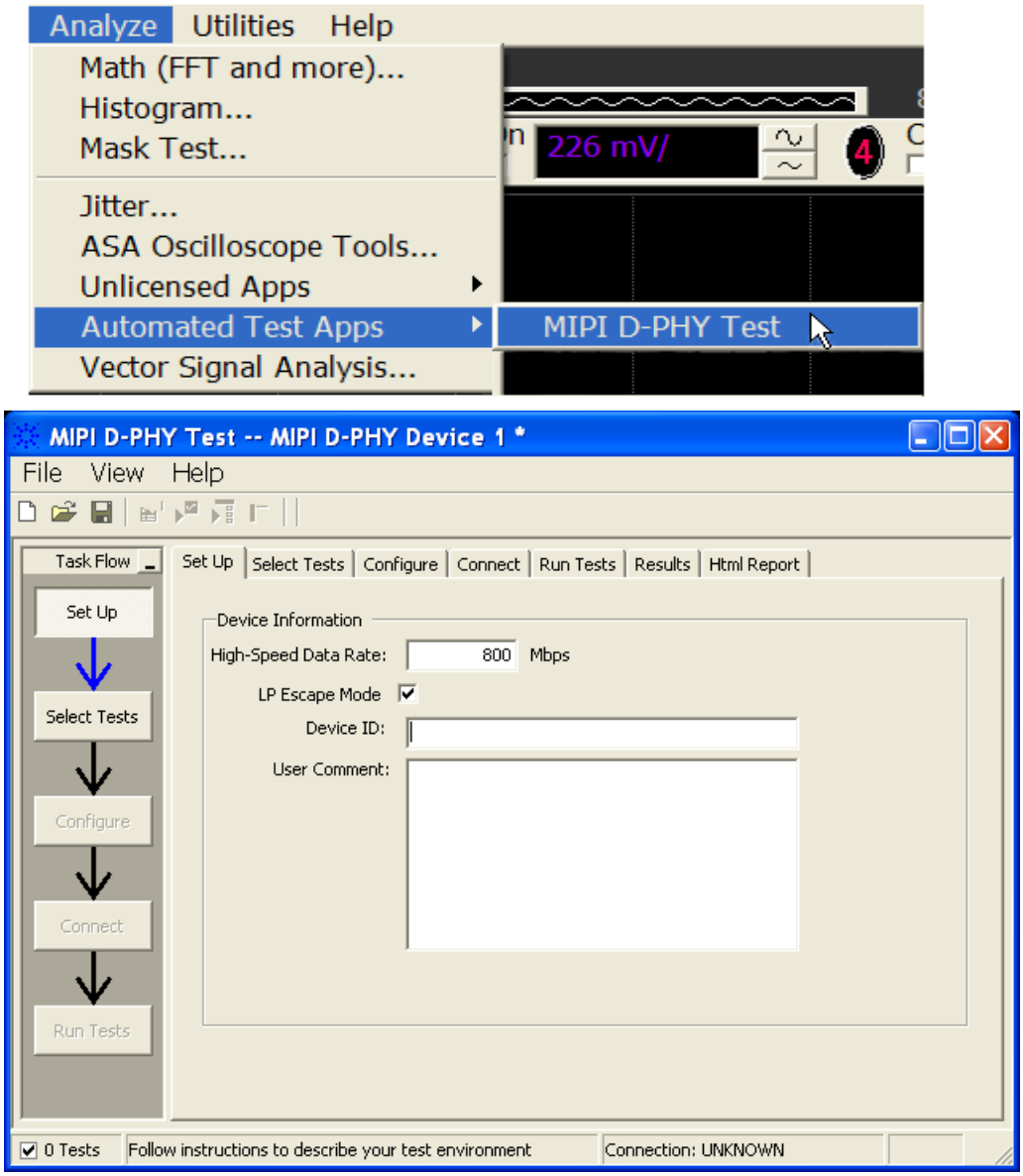

Figure 1 The MIPI D-PHY Conformance Test Application

NOTE If MIPI D-PHY Test does not appear in the Automated Test Apps menu, the MIPI D-PHY Conformance Test Application has not been installed (see Chapter 1, "Installing the MIPI D-PHY Conformance Test Application").

Figure 1 shows the MIPI D-PHY Conformance Test Application main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

Set Up	Lets you identify and setup the test environment, including information about the device under test.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters (like memory depth). This information appears in the HTML report.
Connect	Shows you how to connect the oscilloscope to the device under test for the tests to be run.
Run Tests	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

Online Help Topics

For information on using the MIPI D-PHY Conformance Test Application, see its online help (which you can access by choosing Help>Contents... from the application's main menu).

The MIPI D-PHY Conformance Test Application's online help describes:

- Starting the MIPI D-PHY Conformance Test Application.
  - To view or minimize the task flow pane.
  - To view or hide the toolbar.
- Creating or opening a test project.
- Setting up MIPI D-PHY test environment.
- Selecting tests.

- Configuring selected tests.
- Connecting the oscilloscope to the Device Under Test (DUT).
- Running tests.
- Viewing test results.
  - To show reference images and flash mask hits.
  - To change margin thresholds.
- Viewing/printing the HTML test report.
- Understanding the HTML report.
- Saving test projects.

Part I
Electrical Characteristics

Agilent Technologies

Part I
High Speed Clock Transmitter (HS Clock Tx) Electrical Tests

This section provides the Methods of Implementation (MOIs) for the High Speed Clock Transmitter (HS Clock Tx) Electrical tests using an Agilent 80000, 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Conformance Test Application.

Probing for High Speed Clock Transmitter Electrical Tests

When performing the HS Clock Tx tests, the MIPI D-PHY Conformance Test Application will prompt you to make the proper connections. The connections for the HS Clock Tx tests may look similar to the following diagram. Refer to the Connection tab in MIPI D-PHY Conformance Test application for the exact number of probe connections.

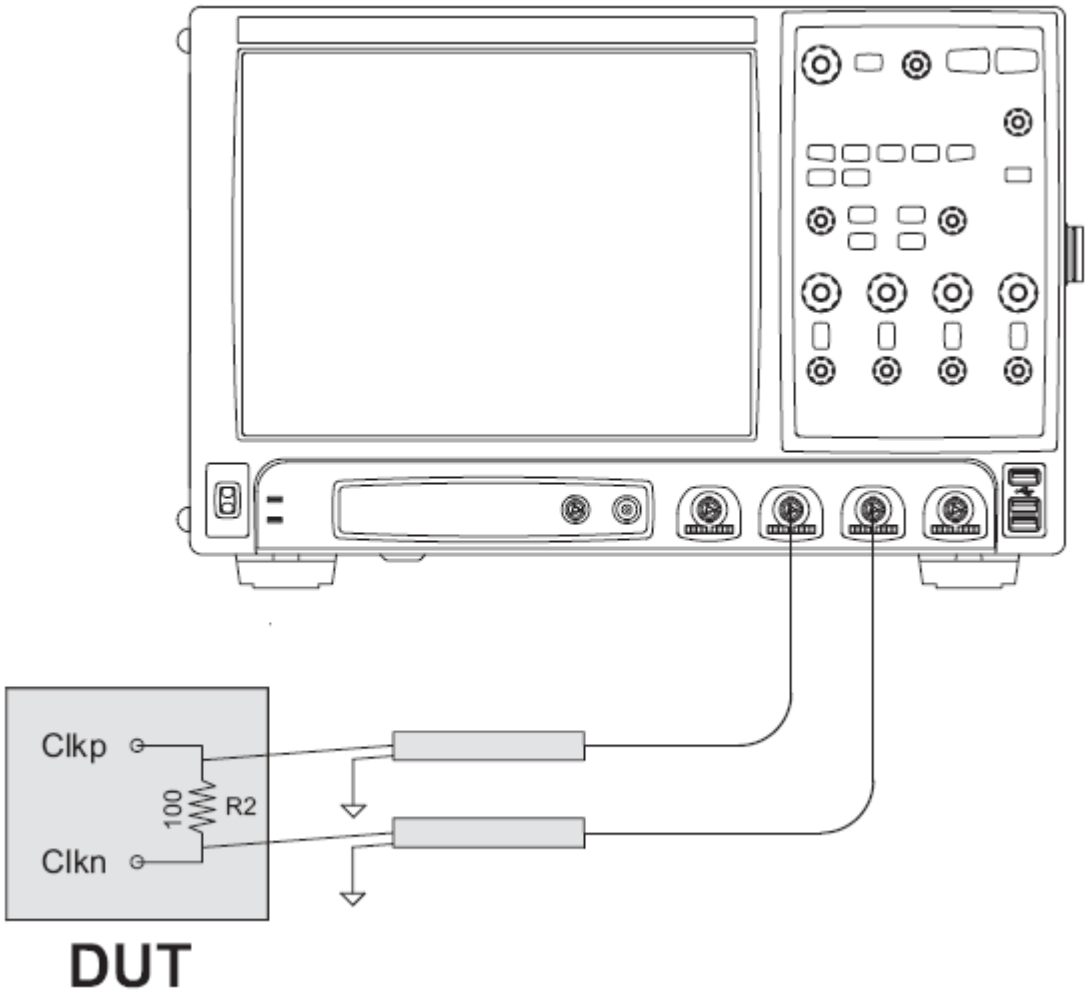

Figure 2 Probing for High Speed Clock Transmitter Electrical Tests

You can identify the channels used for each signal in the Configuration tab of the MIPI D-PHY Conformance Test Application. (The channels shown in Figure 2 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 10, “InfiniiMax Probing,” starting on page 157.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Conformance Test Application" on page 21.

2 In the MIPI D-PHY Conformance Test application, click the Set Up tab.

3 Enter the High-Speed Data Rate, Device ID and User Comments.

4 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

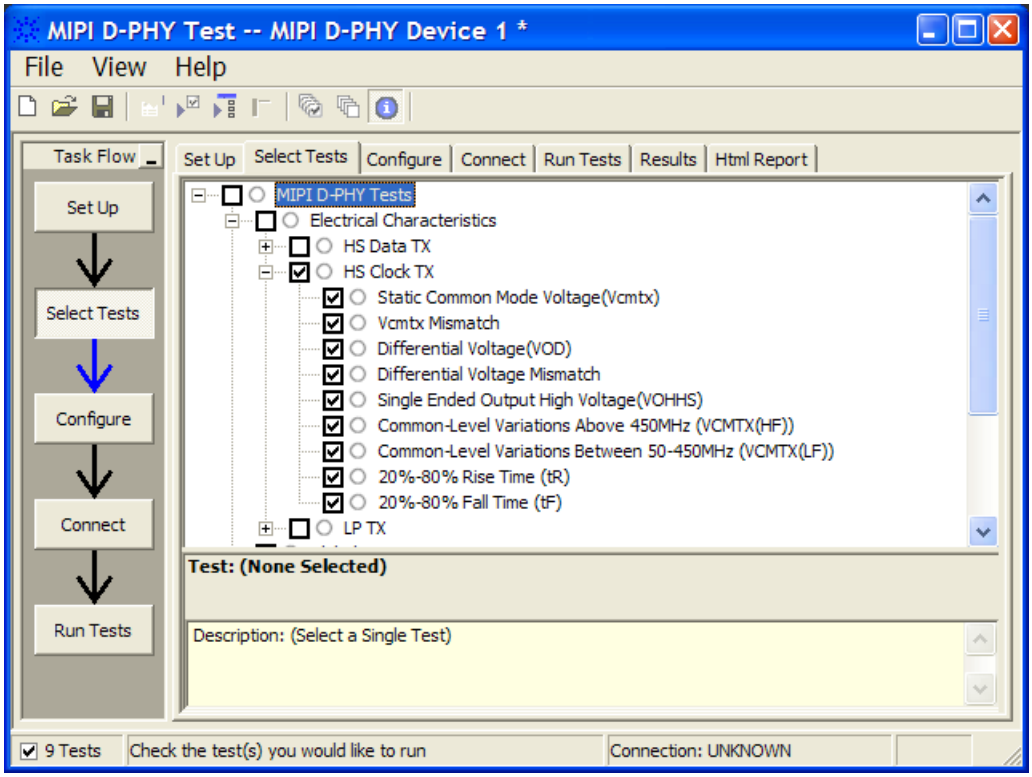

Figure 3 Selecting High Speed Clock Transmitter Electrical Tests

5 Follow the MIPI D-PHY Conformance Test application's task flow to set up the configuration options (see Table 1), run the tests and view the tests results.

Table 1 Test Configuration Options

Configuration Option	Description
Scope Channel Resources	
Dp	Identifies the oscilloscope channels probing Dp signal.
Dn	Identifies the oscilloscope channels probing Dn signal.
CLK(Diff)	Identifies the oscilloscope channels probing clock (differentially).
CLKp	Identifies the oscilloscope channels probing clock.
CLKn	Identifies the oscilloscope channels probing clock.
HS Tests Configuration	
Number of HS Burst	Number of HS burst to be observed in Data and Clock tests. For Clock, if Clock signal doesn't contain LP signal, 2M sample points will be used instead.
LP Trigger Threshold	Trigger level for LP edges. Set it such that it will not trigger wrongly on HS. Possible values are between 0.200 and 0.880. The D-PHY specification recommends 0.550-0.880.
Single-Ended HS Threshold Level	Trigger level for Single-Ended HS edges. This is the voltage level that will be used by the application to determine edges of single-ended HS signal. Possible values are between 0 and 0.650.
Export Tested Waveform Data	Specifies whether to export waveform data that is used in the test. Selecting to export will cause the tests to take slightly longer time to complete.

HS Clock Tx Static Common Mode Test Method of Implementation

The High Speed Clock Transmitter Common-Mode Voltage, V_{CMTX} is defined as the arithmetic mean value of the voltages at the Clkp and Clkn pins. Because of various types of signal distortion that may occur, it is possible for V_{CMTX} to have different values when a Differential-1 vs. Differential-0 state is driven.

For this test, the values for V_{CMTX} are measured for both the Differential-1 and Differential-0 states and averaged.

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2}$$

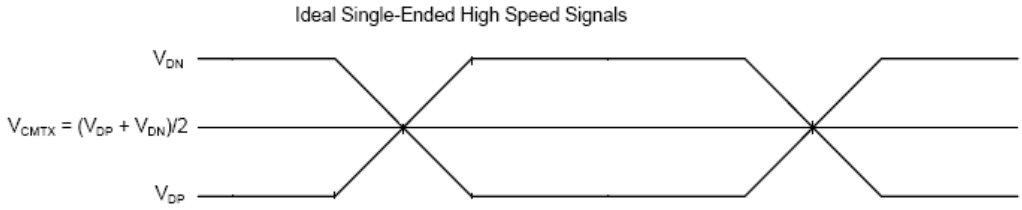

Figure 4 Ideal Single-Ended High Speed Signals

Test Definition Notes from the Specification

Table 2 HS Transmitter DC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
$V_{(CMTX)}$	HS transmit static common-mode voltage	150	200	250	mV	1

NOTE 1: Value when driving into load impedance anywhere in the Z_{ID} range.

PASS Condition

The measured V_{CMTX} value for the test signal must be within the conformance limit as specified in Table 16 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Ensure that the DUT does not go into LP mode during the test.
2. Find the optimized vertical range for Clkp and Clkn.
3. Trigger the oscilloscope to acquire Clkp and Clkn.
4. Construct differential waveform by using the following equation:

   ClkDiff = Clkp-Clkn
5. Construct common-mode waveform by using the following equation:

   ClkCommonMode = (Clkp+Clkn)/2
6. Sample the Common-Mode HS Clock waveform by using the center of the differential HS Clock's UI as sampler and denote as V_{CMTX}.
7. Separate the V_{CMTX} into 2 arrays; V_{CMTX} for Differential-1 and V_{CMTX} for Differential-0 by using the following criteria:

   If average ClkDiff during the UI>0, then V_{CMTX}=>V_{CMTX} for Differential-1.

   If average ClkDiff during the UI<0, then V_{CMTX}=>V_{CMTX} for Differential-0.
8. Report the measurement results:
   a. Mean V_{CMTX} for Differential-1 and Differential-0
   b. V_{CMTX} worst value between Differential-1 and Differential-0
9. Compare the measured V_{CMTX} worst value with the conformance test limits.

Test References

See Table 16 - HS Transmitter DC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

HS Clock Tx Common Mode Mismatch Test Method of Implementation

For this $\Delta V_{CMTX(1,0)}$ test, the values for V_{CMTX} is measured for both the Differential-1 and Differential-0 states and averaged. The difference between the V_{CMTX} values for Differential-1 and Differential-0 is computed.

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2} \quad , \quad \Delta V_{CMTX(1,0)} = \frac{V_{CMTX(1)} - V_{CMTX(0)}}{2}$$

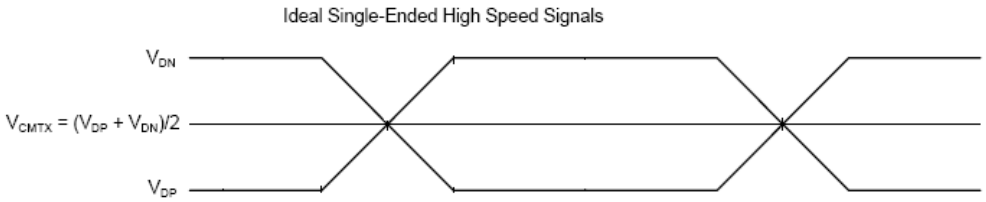

Figure 5 Ideal Single-Ended High Speed Signals

Test Definition Notes from the Specification

Table 3 HS Data Transmitter DC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMTX(1,0)}$	$V_{CMTX(1,0)}$ mismatch when output is Differential-1 or Differential-0	-	-	5	mV	2

NOTE 2: It is recommended the implementer minimize ΔV_{OD} and $\Delta V_{CMTX(1,0)}$ in order to minimize radiation and optimize integrity.

PASS Condition

The measured $\Delta V_{CMTX(1,0)}$ value for the test signal must be within the conformance limit as specified in Table 16 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1 This test requires the following pre-requisite tests.

   a HS Clock Tx Static Common Mode Voltage (V_{CMTX})

   b The actual V_{CMTX} for Differential-1 and Differential-0 measurements are performed and test results are stored.

2 Calculate the difference between V_{CMTX} for Differential-1 and Differential-0.

3 Report the measurement results.

V_{CMTX} for Differential-1 and Differential-0

4 Compare the measured ΔV_{CMTX} between Differential-1 and Differential-0 value with the conformance test limit.

Test References

See Table 16 - HS Transmitter DC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

HS CLock Tx Differential Voltage Test Method of Implementation

The Output Differential Voltage, V_{OD} is defined as the difference of voltages V_{DP} and V_{DN} at the Dp and Dn pins, respectively.

$$V_{OD} = V_{DP} - V_{DN}$$

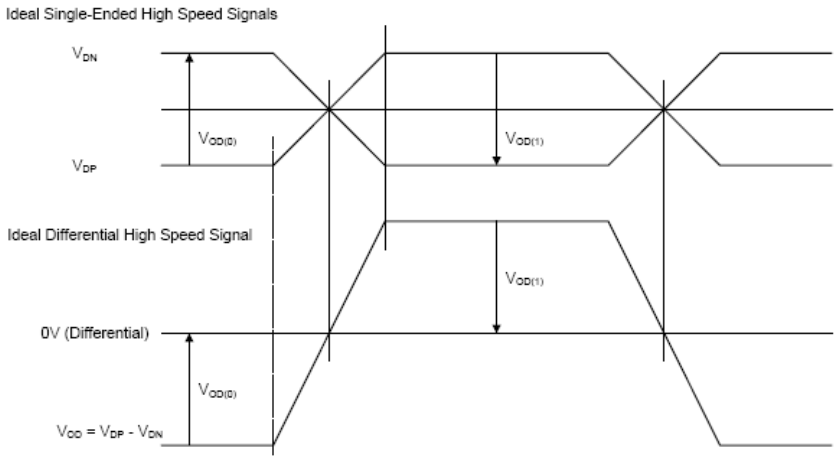

Figure 6 Ideal Single-Ended and Differential High Speed Signals

Test Definition Notes from the Specification

Table 4 HS Data Transmitter DC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
V_{OD}	HS transmit differential voltage	140	200	270	mV	1

NOTE 1: Value when driving into load impedance anywhere in the Z_{ID} range.

PASS Condition

The measured V_{OD} value for the test signal must be within the conformance limit as specified in Table 16 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Ensure that the DUT does not go into LP mode during the test.
2. Find the optimized vertical range for Clkp and Clkn.
3. Trigger the oscilloscope to acquire Clkp and Clkn.
4. Sample the differential HS Clock waveform by using middle of the differential HS Clock's UI as sampler and denote as V_{OD}.
5. Use the same sampler to sample the voltage level at Clkp and Clkn. Each sampled voltage value is denoted as V_{CLKP} and V_{CLKN} respectively.
6. Separate the V_{OD} into 2 arrays; V_{OD} for Differential-1 and V_{OD} for Differential-0 by using the following criteria:

   If $V_{CLKP}>V_{CLKN}$, then $V_{OD}=>V_{OD}$ for Differential-1

   If $V_{CLKP}<V_{CLKN}$, then $V_{OD}=>V_{OD}$ for Differential-0
7. Report the measurement results:
   a. Mean V_{OD} for Differential-1 and Differential-0
   b. V_{OD} worst value between Differential-1 and Differential-0
8. Compare the measured V_{OD} worst value with the conformance test limits.

Test References

See Table 16 - HS Transmitter DC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

HS Clock Tx Differential Voltage Mismatch Test Method of Implementation

The Output Differential Voltage Mismatch, ΔV_{OD} is defined as the difference of the absolute values of the differential output voltage in the Differential-1 state $V_{OD(1)}$ and the differential output voltage in the Differential-0 state $V_{OD(0)}$.

$$\Delta V_{OD} = \left|V_{OD(1)}\right| - \left|V_{OD(0)}\right|$$

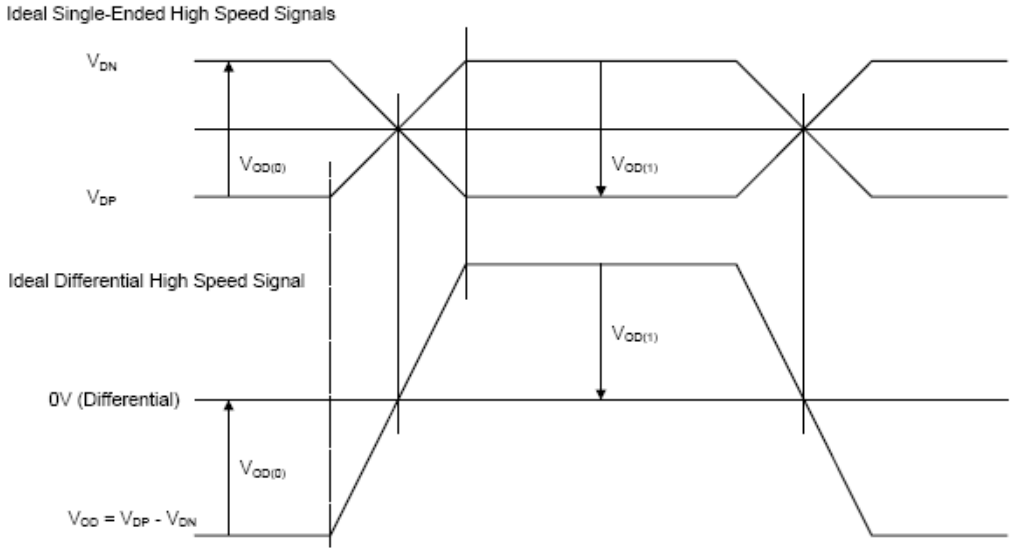

Figure 7 Ideal Single-Ended and Differential High Speed Signals

Test Definition Notes from the Specification

Table 5 HS Data Transmitter DC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
$\lvert\Delta V_{OD}\rvert$	V_{OD} mismatch when output is Differential-1 or Differential-0			10	mV	2

NOTE 2: It is recommended the implementer minimize ΔV_{OD} and $\Delta V_{CMTX(1,0)}$ in order to minimize radiation and optimize signal integrity.

PASS Condition

The measured V_{OD} value for the test signal must be within the conformance limit as specified in Table 16 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. This test requires the following pre-requisite tests.
   a. HS Clock Tx Differential Voltage (V_{OD})
   b. The actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
2. Calculate the difference between V_{OD} for Differential-1 and Differential-0.
3. Report the measurement results.
   a. V_{OD} for Differential-1 and Differential-0
4. Compare the measured ΔV_{OD} between Differential-1 and Differential-0 value with the conformance test limit.

Test References

See Table 16 - HS Transmitter DC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

HS Clock Tx Single-Ended Output High Voltage Test Method of Implementation

The output voltages V_{DP} and V_{DN} at the Clkp and Clkn pins should not exceed the High-Speed Output High Voltage, V_{OHHS}. V_{OLHS} is the High-Speed Output Low Voltage on Clkp and Clkn and is determined by V_{OD} and V_{CMTX}. The High-Speed V_{OUT} is bounded by the minimum value of V_{OLHS} and the maximum value of V_{OHHS}.

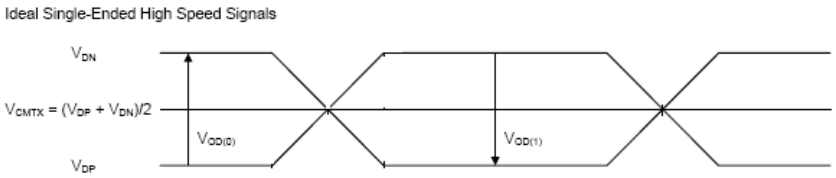

Figure 8 Ideal Single-Ended High Speed Signals

Test Definition Notes from the Specification

Table 6 HS Data Transmitter DC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
V_{OHHS}	HS output high voltage			360	mV	1

NOTE 1: Value when driving into load impedance anywhere in the Z_{ID} range.

PASS Condition

The measured V_{OHHS} value for the test signal must be within the conformance limit as specified in Table 16 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Ensure that the DUT does not go into LP mode during the test.
2. Find the optimized vertical range for Clkp and Clkn.
3. Trigger the oscilloscope to acquire Clkp and Clkn.
4. Measure the maximum voltage value for each single-ended HS Clock signal and denote each value as $V_{OHHS(CLKP)}$ and $V_{OHHS(CLKN)}$.

5 Report the measurement results:
   a V_{OHHS} (Clkp)
   b V_{OHHS} (Clkn)
   c Worst V_{OHHS} value
6 Compare the measured V_{OHHS} value with the conformance test limit.

Test References

See Table 16 - HS Transmitter DC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

HS Clock Tx Common-Level Variations Above 450 MHz Test Method of Implementation

For this $\Delta V_{CMTX(HF)}$ test, the common mode voltage, V_{CMTX} is obtained by using the following equation:

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2}$$

Ideally, the common mode voltage should be as shown in Figure 9. In reality, various types of distortion could take place, as shown in Figure 10.

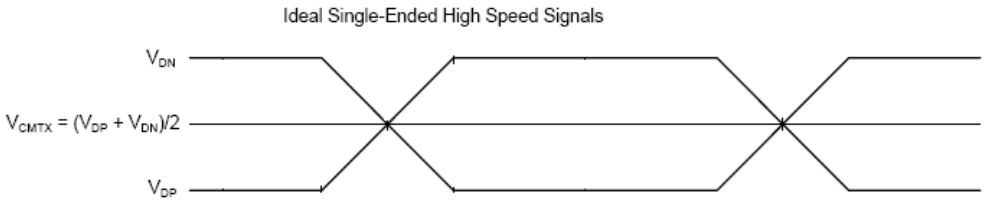

Figure 9 Ideal Single-Ended High Speed Signals

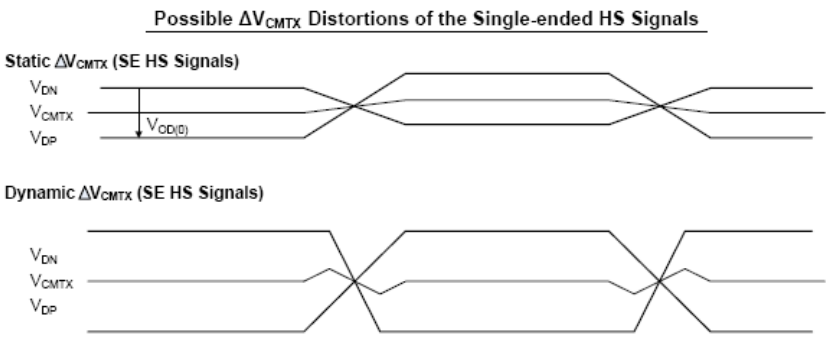

Figure 10 Possible Distortions of the ΔV_{CMTX} Single-Ended High Speed Signals

Test Definition Notes from the Specification

Table 7 HS Data Transmitter AC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMTX(HF)}$	Common-level variations above 450MHz			15	mV_{RMS}	

PASS Condition

The measured $\Delta V_{CMTX(HF)}$ value for the test signal must be within the conformance limit as specified in Table 17 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Ensure that the DUT does not go into LP mode during the test.
2. Find the optimized vertical range for Clkp and Clkn.
3. Trigger the oscilloscope to acquire Clkp and Clkn.
4. Construct common-mode waveform using the following equation:

   ClkCommonMode = (Clkp+Clkn)/2
5. Apply an 8th-order Butterworth IIR bandpass filter, with a cutoff frequency of 450 MHz, to the common-mode waveform.
6. Measure the RMS voltage for the filtered waveform and record as $\Delta V_{CMTX(HF)}$.
7. Report the measurement results:
   a. $\Delta V_{CMTX(HF)}$ value
8. Compare the measured $\Delta V_{CMTX(HF)}$ value with the conformance test limit.

Test References

See Table 17 - HS Transmitter AC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

HS Clock Tx Common-Level Variations Between 50-450 MHz Test Method of Implementation

For this $\Delta V_{CMTX(LF)}$ test, the common mode voltage V_{CMTX} is obtained by using the following equation:

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2}$$

Ideally, the common mode voltage should be as shown in Figure 11. In reality, various types of distortion could take place, as shown in Figure 12.

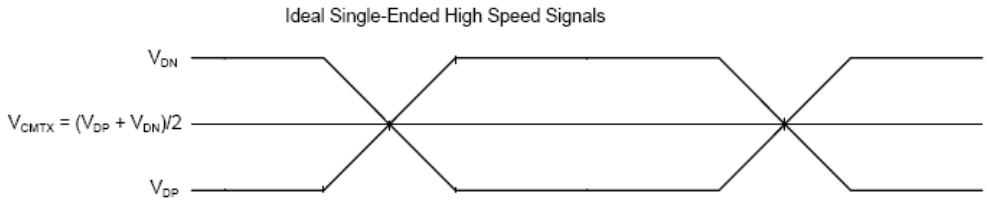

Figure 11 Ideal Single-Ended High Speed Signals

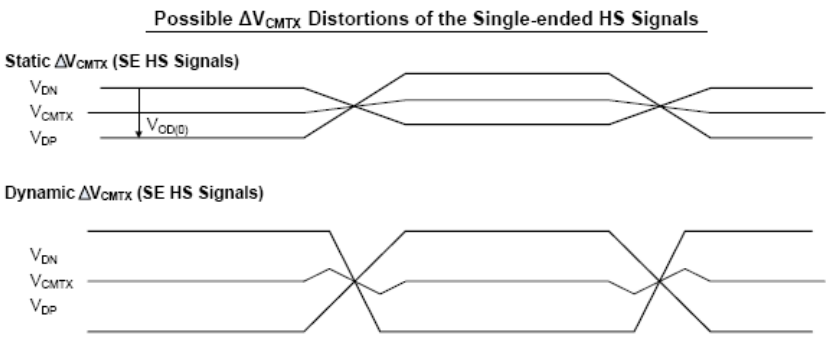

Figure 12 Possible Distortions of the ΔV_{CMTX} Single-Ended High Speed Signals

Test Definition Notes from the Specification

Table 8 HS Data Transmitter AC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMTX(LF)}$	Common-level variation between 50-450 MHz			25	mV_{PEAK}	

PASS Condition

The measured $\Delta V_{CMTX(LF)}$ value for the test signal must be within the conformance limit as specified in Table 17 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Ensure that the DUT does not go into LP mode during the test.
2. Find the optimized vertical range for Clkp and Clkn.
3. Trigger the oscilloscope to acquire Clkp and Clkn.
4. Construct common-mode waveform by using the following equation:

   ClkCommonMode = (Clkp+Clkn)/2
5. Apply an 8th-order Butterworth IIR bandpass filter, with –3dB cutoff frequencies of 50 and 450 MHz, to the common-mode waveform.
6. Measure the min and max voltage for the filtered waveform.
7. Select the worst absolute value for the min and max voltage and record it as $\Delta V_{CMTX(LF)}$.
8. Report the measurement results:
   a. $\Delta V_{CMTX(LF)}$ value
9. Compare the measured $\Delta V_{CMTX(LF)}$ value with the conformance test limit.

Test References

See Table 17 - HS Transmitter AC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

HS Clock Tx 20%-80% Rise Time Test Method of Implementation

The rise time, t_R is defined as the transition time between 20% and 80% of the full HS signal swing. The driver must meet the t_R specifications for all allowable Z_{ID}.

Test Definition Notes from the Specification

Table 9 HS Data Transmitter AC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
t_R and t_F	20%-80% rise time and fall time			0.3	UI	1
		150			ps	

NOTE 1: UI is equal to 1/(2*fh).

The frequency 'fh' is the highest fundamental frequency for data transmission and is equal to $1/(2*UI_{INST,\ MIN})$. Implementers shall specify a value $UI_{INST,\ MIN}$ that represents the minimum instantaneous UI possible within a high speed data transfer for a given implementation.

PASS Condition

The measured t_R value for the test signal must be within the conformance limit as specified in Table 17 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. This test requires the following pre-requisite tests:
   a. HS Clock Tx Differential Voltage (V_{OD})
   b. The actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
2. Ensure that the DUT does not go into LP mode during the test.
3. Find the optimized vertical range for Clkp and Clkn.
4. Trigger the oscilloscope to acquire Clkp and Clkn.
5. Construct differential waveform by using the following equation:

   ClkDiff = Clkp-Clkn
6. Define the measurement threshold as:

   Top Level: V_{OD} for Differential-1

   Base Level: V_{OD} for Differential-0

7 Measure all 20%-80% rise time at all rising edges that meet the 20%-80% threshold criteria and record the values.

8 Report the measurement results:

   a t_R (Max)

   b t_R (Min)

   c t_R (Mean)

9 Compare the measured t_R (Mean) with the conformance test limit.

Test References

See Table 17 - HS Transmitter AC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

HS Clock Tx 20%-80% Fall Time Test Method of Implementation

The rise time, t_F is defined as the transition time between 20% and 80% of the full HS signal swing. The driver must meet the t_F specifications for all allowable Z_{ID}.

Test Definition Notes from the Specification

Table 10 HS Data Transmitter AC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
t_R and t_F	20%-80% rise time and fall time			0.3	UI	1
		150			ps	

NOTE 1: UI is equal to 1/(2*fh).

The frequency 'fh' is the highest fundamental frequency for data transmission and is equal to $1/(2*UI_{INST,\ MIN})$. Implementers shall specify a value $UI_{INST,\ MIN}$ that represents the minimum instantaneous UI possible within a high speed data transfer for a given implementation.

PASS Condition

The measured t_F value for the test signal must be within the conformance limit as specified in Table 17 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. This test requires the following pre-requisite tests:
   a. HS Clock Tx Differential Voltage (V_{OD})
   b. The actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.
2. Ensure that the DUT does not go into LP mode during the test.
3. Find the optimized vertical range for Clkp and Clkn.
4. Trigger the oscilloscope to acquire Clkp and Clkn.
5. Construct differential waveform by using the following equation:

   ClkDiff = Clkp-Clkn
6. Define the measurement threshold as:

   Top Level: V_{OD} for Differential-1

   Base Level: V_{OD} for Differential-0

7 Measure all 20%-80% rise time at all falling edges that meet the 20%-80% threshold criteria and record the values.

8 Report the measurement results:

   a t_F (Max)

   b t_F (Min)

   c t_F (Mean)

9 Compare the measured t_F (Mean) with the conformance test limit

Test References

See Table 17 - HS Transmitter AC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

3 High Speed Data Transmitter (HS Data Tx) Electrical Tests

This section provides the Methods of Implementation (MOIs) for the High Speed Data Transmitter (HS Data Tx) Electrical tests using an Agilent 80000, 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Conformance Test Application.

Probing for High Speed Data Transmitter Electrical Tests

When performing the HS Data Tx tests, the MIPI D-PHY Conformance Test Application will prompt you to make the proper connections. The connections for the HS Data Tx tests may look similar to the following diagrams. Refer to the Connection tab in MIPI D-PHY Conformance Test application for the exact number of probe connections.

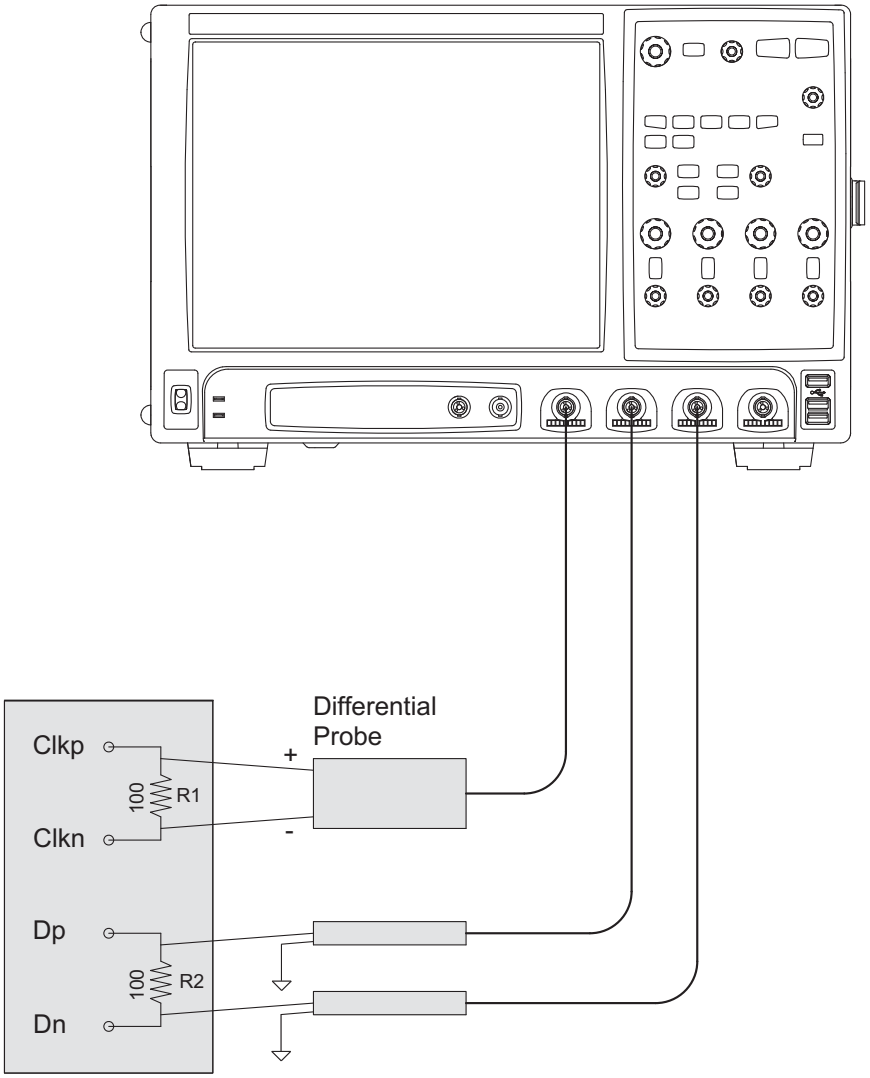

Figure 13 Probing with Three Probes for High Speed Data Transmitter Electrical Tests

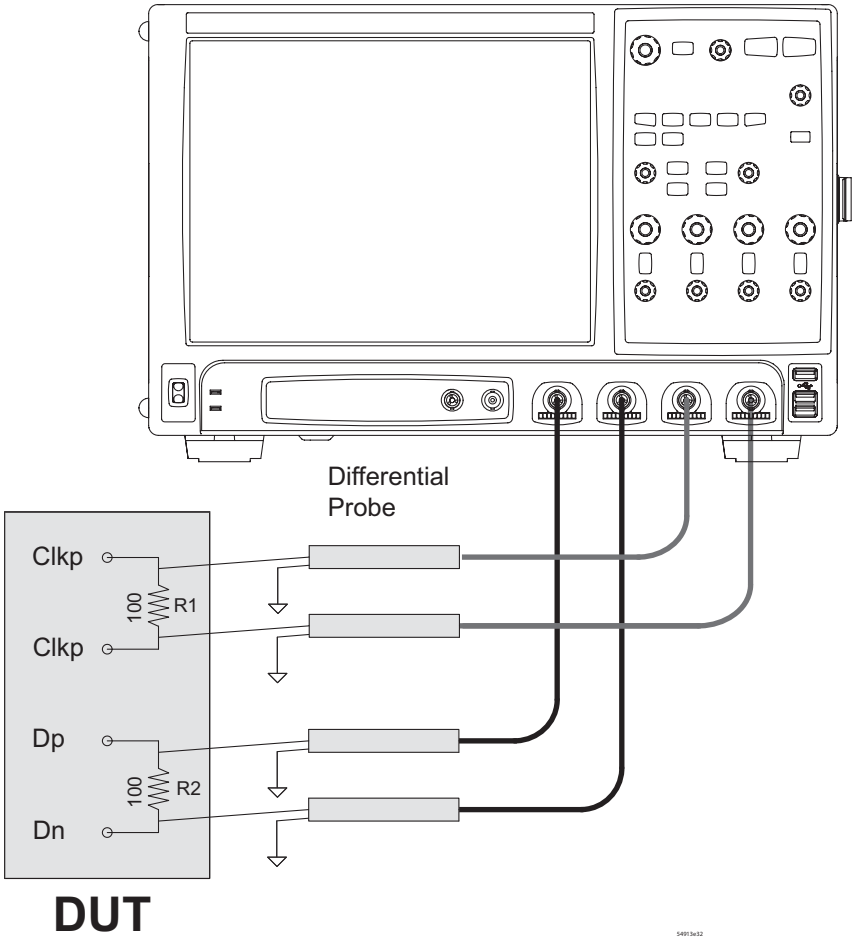

Figure 14 Probing with Four Probes for High Speed Data Transmitter Electrical Tests

You can identify the channels used for each signal in the Configuration tab of the MIPI D-PHY Conformance Test Application. (The channels shown in Figure 13 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 10, “InfiniiMax Probing,” starting on page 157.

Test Procedure

1. Start the automated test application as described in “Starting the MIPI D-PHY Conformance Test Application" on page 21.
2. In the MIPI D-PHY Conformance Test application, click the Set Up tab.
3. Enter the High-Speed Data Rate, Device ID and User Comments.
4. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

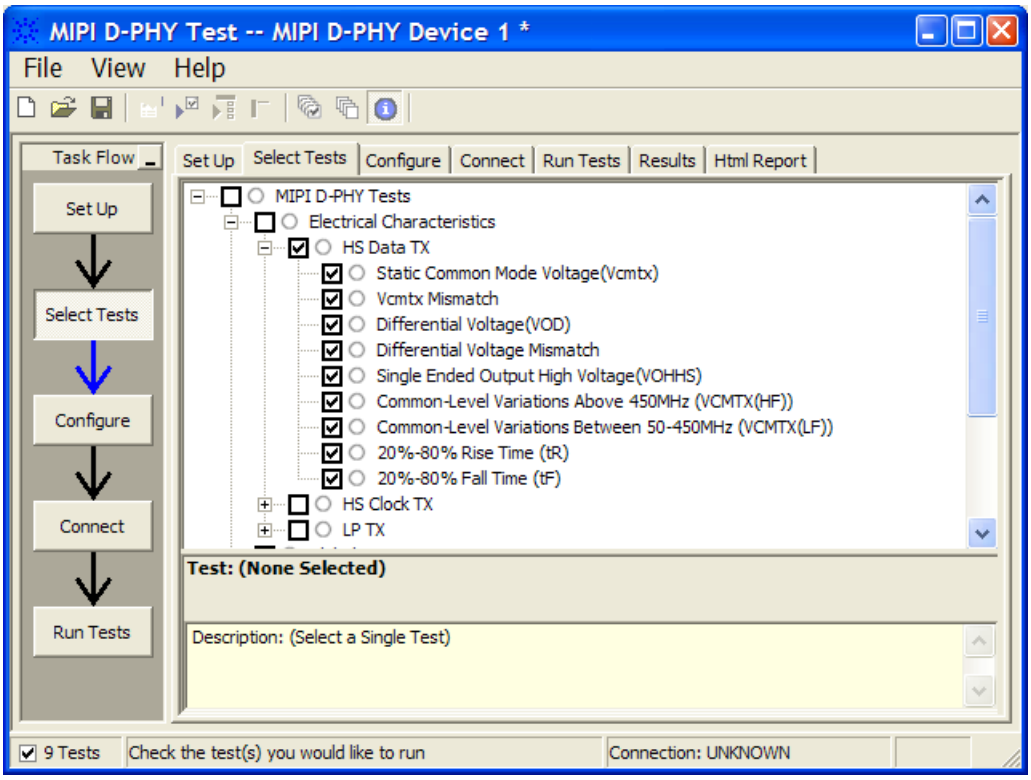

Figure 15 Selecting High Speed Data Transmitter Electrical Tests

5 Follow the MIPI D-PHY Conformance Test application's task flow to set up the configuration options (see Table 11), run the tests and view the tests results.

Table 11 Test Configuration Options

Configuration Option	Description
Scope Channel Resources	
Dp	Identifies the oscilloscope channels probing Dp signal.
Dn	Identifies the oscilloscope channels probing Dn signal.
CLK(Diff)	Identifies the oscilloscope channels probing clock (differentially).
CLKp	Identifies the oscilloscope channels probing clock.
CLKn	Identifies the oscilloscope channels probing clock.
HS Tests Configuration	
Number of HS Burst	Number of HS burst to be observed in Data and Clock tests. For Clock, if Clock signal doesn't contain LP signal, 2M sample points will be used instead.
LP Trigger Threshold	Trigger level for LP edges. Set it such that it will not trigger wrongly on HS. Possible values are between 0.200 and 0.880. The D-PHY specification recommends 0.550-0.880.
Single-Ended HS Threshold Level	Trigger level for Single-Ended HS edges. This is the voltage level that will be used by the application to determine edges of single-ended HS signal. Possible values are between 0 and 0.650.
Export Tested Waveform Data	Specifies whether to export waveform data that is used in the test. Selecting to export will cause the tests to take slightly longer time to complete.
Electrical Characteristics	
HS Data Tx	
HS Full Dynamic Range	To enable or disable the use of full dynamic range when measuring HS data electrical characteristic. LP trigger threshold will be changed when this feature is turned on.
Transition Time Measurement Upper Threshold	Specifies in percentage the upper measurement threshold for transition time measurement.
Transition Time Measurement Lower Threshold	Specifies in percentage the lower measurement threshold for transition time measurement.

HS Data Tx Static Common Mode Test Method of Implementation

The High Speed Data Transmitter Static Common-Mode Voltage, V_{CMTX} is defined as the arithmetic mean value of the voltages at the Dp and Dn pins. Because of various types of signal distortion that may occur, it is possible for V_{CMTX} to have different values when a Differential-1 vs. Differential-0 state is driven.

For this test, the values for V_{CMTX} is measured for both the Differential-1 and Differential-0 states and averaged over at least 10,000 observations.

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2}$$

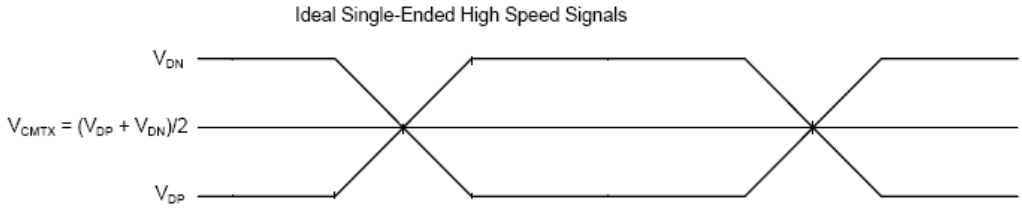

Figure 16 Ideal Single-Ended High Speed Signals

Test Definition Notes from the Specification

Table 12 HS Transmitter DC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
$V_{(CMTX)}$	HS transmit static common-mode voltage	150	200	250	mV	1

NOTE 1: Value when driving into load impedance anywhere in the Z_{ID} range.

PASS Condition

The measured V_{CMTX} value for the test signal must be within the conformance limit as specified in Table 16 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1 Trigger at SoT of HS Data burst (LP11 to LP01).

2 Place the triggered edges on the left of the screen.

3 If Full HS Dynamic Range is configured, a pre-requisite step is executed to find the most optimized vertical dynamic range for HS Data burst.

4 Find the HS Data bursts. Depending on the number of HS Data burst configuration; if the current acquisition does not have enough HS Data burst, more acquisitions are required.

5 Collect all the required HS Data and HS Clock signal.

6 For the HS Data, common-mode waveform is required. The waveform can be constructed by using the following equation:

DataCommonMode = (Dp+Dn)/2

7 For the HS Clock, differential waveform is required. This can be achieved by directly probing the differential signal or by probing the single-ended clock signal and form a differential signal by using the singled-ended signals with the following equation:

ClockDiff = Clkp - Clkn

8 Sample the Common-Mode HS Data waveform by using all the edges of the differential HS Clock as sampler and denote it as V_{CMTX}.

9 At the same time, sample the voltage level at single-ended HS Data signal and denote as V_{DP} and V_{DN}.

10 Separate the V_{CMTX} into 2 arrays; V_{CMTX} for Differential-1 and V_{CMTX} for Differential-0 by using the following criteria:

If $V_{DP} > V_{DN}$, V_{CMTX} => V_{CMTX} for Differential-1

If $V_{DP} < V_{DN}$, V_{CMTX} => V_{CMTX} for Differential-0

11 Report the measurement results:

- Mean V_{CMTX} for Differential-1 and Differential-0
- V_{CMTX} worst value between Differential-1 and Differential-0

12 Compare the measured V_{CMTX} worst value with the conformance test limit.

Test References

See Table 16 - HS Transmitter DC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

HS Data Tx Common Mode Mismatch Test Method of Implementation

For this $\Delta V_{CMTX(1,0)}$ test, the values for V_{CMTX} is measured for both the Differential-1 and Differential-0 states and averaged over at least 10,000 observations. The difference between the V_{CMTX} values for Differential-1 and Differential-0 is computed.

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2} \quad , \quad \Delta V_{CMTX(1,0)} = \frac{V_{CMTX(1)} - V_{CMTX(0)}}{2}$$

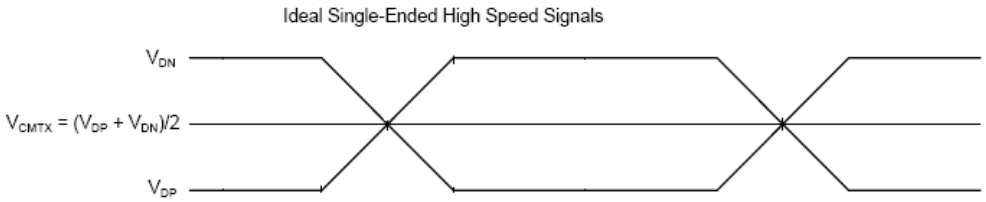

Figure 17 Ideal Single-Ended High Speed Signals

Test Definition Notes from the Specification

Table 13 HS Data Transmitter DC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMTX(1,0)}$	$V_{CMTX(1,0)}$ mismatch when output is Differential-1 or Differential-0	-	-	5	mV	2

NOTE 2: It is recommended the implementer minimize ΔV_{OD} and $\Delta V_{CMTX(1,0)}$ in order to minimize radiation and optimize integrity.

PASS Condition

The measured $\Delta V_{CMTX(1,0)}$ value for the test signal must be within the conformance limit as specified in Table 16 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1 This test requires the following pre-requisite tests:

- HS TX Static Common Mode Voltage (VCMTX) (Test ID: 811)
- Actual V_{CMTX} for Differential-1 and Differential-0 measurements are performed and test results are stored.

2 Calculate the difference between V_{CMTX} for Differential-1 and Differential-0.

3 Report the measurement results:

- V_{CMTX} for Differential-1 and Differential-0

4 Compare the measured ΔV_{CMTX} between Differential-1 and Differential-0 value with the conformance test limit.

Test References

See Table 16 - HS Transmitter DC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

HS Data Output Differential Voltage Test Method of Implementation

The Output Differential Voltage, V_{OD} is defined as the difference of voltages V_{DP} and V_{DN} at the Dp and Dn pins, respectively.

$$V_{OD} = V_{DP} - V_{DN}$$

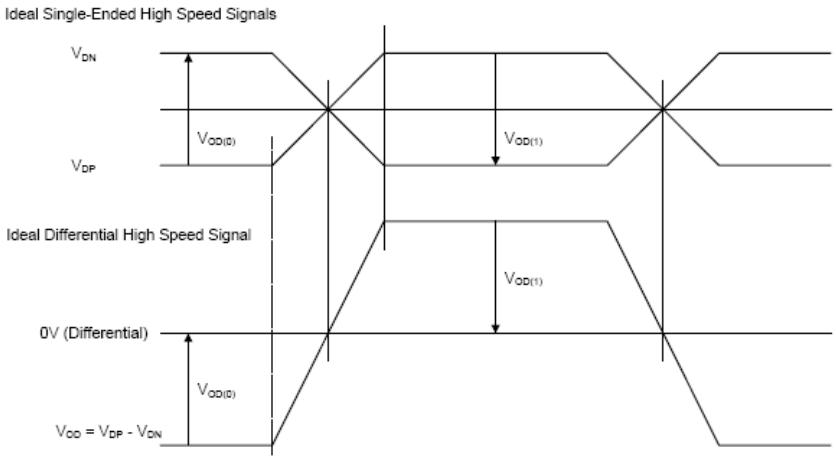

Figure 18 Ideal Single-Ended and Differential High Speed Signals

Test Definition Notes from the Specification

Table 14 HS Data Transmitter DC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
$\lvert V_{OD} \rvert$	HS transmit differential voltage	140	200	270	mV	1

NOTE 1: Value when driving into load impedance anywhere in the Z_{ID} range.

PASS Condition

The measured V_{OD} value for the test signal must be within the conformance limit as specified in Table 16 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1 Trigger at SoT of HS Data burst (LP11 to LP01).

2 Place the triggered edges on the left of the screen.

3 If Full HS Dynamic Range is configured, a pre-requisite step is executed to find the most optimized vertical dynamic range for HS Data burst.

4 Find the HS Data bursts. Depending on the number of HS Data burst configuration; if the current acquisition does not have enough HS Data burst, more acquisitions are required.

5 Collect all the required HS Data and HS Clock signal.

6 For the HS Data, common-mode waveform is required. The waveform can be constructed by using the following equation:

DataDiff = Dp-Dn

7 For the HS Clock, differential waveform is required. This can be achieved by directly probing the differential signal or by probing the single-ended clock signal and form a differential signal by using the singled-ended signals with the following equation:

ClockDiff = Clkp - Clkn

8 Sample the Differential HS Data signal by using all the edges of the differential HS Clock as sampler and denote it as V_{OD}.

9 At the same time, sample the voltage level at the single-ended HS Data signal and denote as V_{DP} and V_{DN}. Note that D-PHY is running at double data rate, thus all edges of HS Clock is taken into account.

10 Separate the V_{OD} into 2 arrays; V_{OD} for Differential-1 and V_{OD} for Differential-0 by using the following criteria:

If $V_{DP} > V_{DN}$, V_{OD} => V_{OD} for Differential-1

If $V_{DP} < V_{DN}$, V_{OD} => V_{OD} for Differential-0

11 Report the measurement results:

- Mean V_{OD} for Differential-1 and Differential-0
- V_{OD} worst value between Differential-1 and Differential-0

12 Compare the measured worst V_{OD} value with the conformance test limit.

Test References

See Table 16 - HS Transmitter DC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

HS Data Output Differential Voltage Mismatch Test Method of Implementation

The Output Differential Voltage Mismatch, ΔV_{OD} is defined as the difference of the absolute values of the differential output voltage in the Differential-1 state $V_{OD(1)}$ and the differential output voltage in the Differential-0 state $V_{OD(0)}$.

$$\Delta V_{OD} = \left|V_{OD(1)}\right| - \left|V_{OD(0)}\right|$$

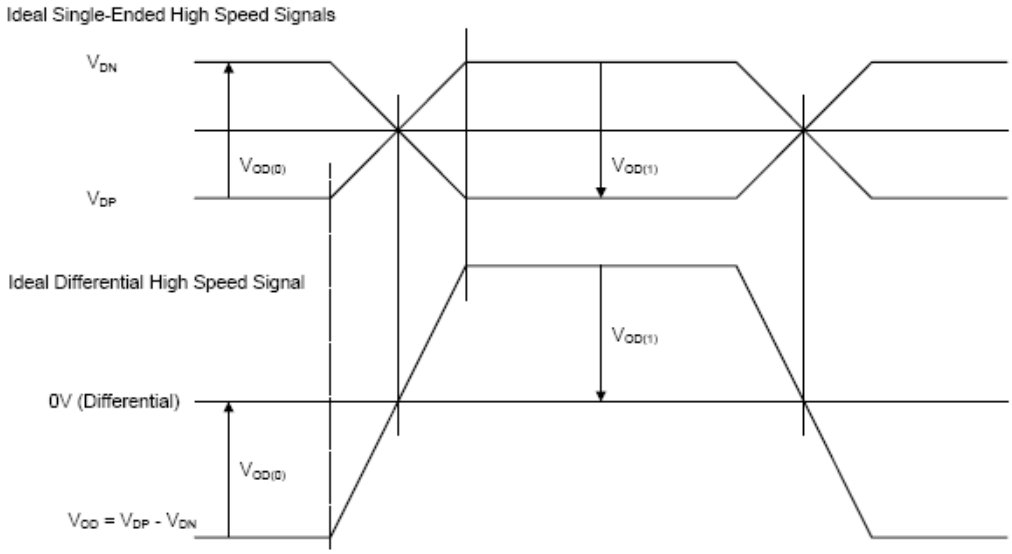

Figure 19 Ideal Single-Ended and Differential High Speed Signals

Test Definition Notes from the Specification

Table 15 HS Data Transmitter DC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
$\lvert\Delta V_{OD}\rvert$	V_{OD} mismatch when output is Differential-1 or Differential-0			10	mV	2

NOTE 2: It is recommended the implementer minimize ΔV_{OD} and $\Delta V_{CMTX(1,0)}$ in order to minimize radiation and optimize signal integrity.

PASS Condition

The measured ΔV_{OD} value for the test signal must be within the conformance limit as specified in Table 16 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1 This test requires the following pre-requisite tests:
   - HS Data Tx Differential Voltage (V_{OD})
   - The actual V_{OD} for Differential-1 and Differential-0 measurements are performed and test results are stored.

2 Calculate the difference between V_{OD} for Differential-1 and Differential-0.

3 Report the measurement results:
   - V_{OD} for Differential-1 and Differential-0

4 Compare the measured ΔV_{OD} between Differential-1 and Differential-0 value with the conformance test limit.

Test References

See Table 16 - HS Transmitter DC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

HS Data Tx Single-Ended Output High Voltage Test Method of Implementation

The output voltages V_{DP} and V_{DN} at the Dp and Dn pins should not exceed the High-Speed Output High Voltage, V_{OHHS}. V_{OLHS} is the High-Speed Output Low Voltage on Dp and Dn, and is determined by V_{OD} and V_{CMTX}. The High-Speed V_{OUT} is bounded by the minimum value of V_{OLHS} and the maximum value of V_{OHHS}.

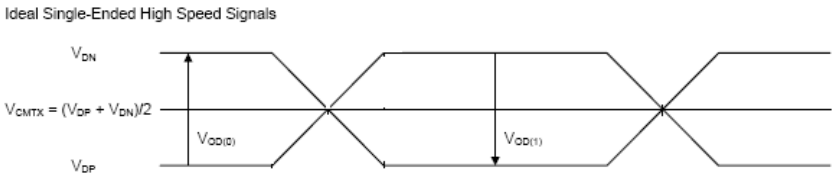

Figure 20 Ideal Single-Ended High Speed Signals

Test Definition Notes from the Specification

Table 16 HS Data Transmitter DC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
V_{OHHS}	HS output high voltage			360	mV	1

NOTE 1: Value when driving into load impedance anywhere in the Z_{ID} range.

PASS Condition

The measured V_{OHHS} value for the test signal must be within the conformance limit as specified in Table 16 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Trigger at SoT of HS Data burst (LP11 to LP01).
2. Place the triggered edges on the left of the screen.
3. If Full HS Dynamic Range is configured, a pre-requisite step is executed to find the most optimized vertical dynamic range for the HS Data burst.
4. Find the HS Data bursts. Depending on the number of HS Data burst configuration; if the current acquisition does not have enough HS Data burst, more acquisitions are required.

5 Collect all the required HS Data.

6 Measure the maximum voltage value for each single-ended HS Data signal and denote each value as $V_{OHHS}(Dp)$ and $V_{OHHS}(Dn)$.

7 Perform the signal conditioning for the clock signal channel.

8 Report the measurement results:

- $V_{OHHS}(Dp)$
- $V_{OHHS}(Dn)$
- Worst V_{OHHS} value

9 Compare the measured V_{OHHS} worst value with the conformance test limit.

Test References

See Table 16 - HS Transmitter DC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

HS Data Tx Common Level Variations Above 450 MHz Test Method of Implementation

The Common-Mode Voltage, V_{CMTX} is defined as the arithmetic mean value of the voltages at the Dp and Dn pins. Because of various types of signal distortion that may occur, it is possible for V_{CMTX} to have different values when a Differential-1 vs. Differential-0 state is driven.

For this $\Delta V_{CMTX(HF)}$ test, the values for V_{CMTX} is obtained by using the following equation:

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2}$$

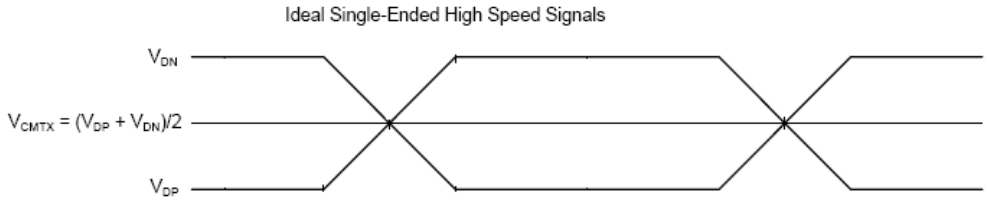

Figure 21 Ideal Single-Ended High Speed Signals

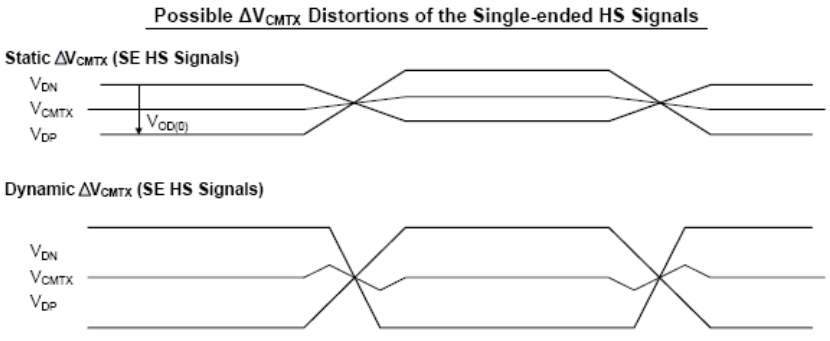

Figure 22 Possible Distortions of the ΔV_{CMTX} Single-Ended High Speed Signals

Test Definition Notes from the Specification

Table 17 HS Data Transmitter AC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMTX(HF)}$	Common-level variations above 450MHz			15	mV_{RMS}	

PASS Condition

The measured $\Delta V_{CMTX(HF)}$ value for the test signal must be within the conformance limit as specified in Table 17 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Trigger at SoT of HS Data burst (LP11 to LP01).
2. Place the triggered edges on the left of the screen.
3. If Full HS Dynamic Range is configured, a pre-requisite step is executed to find the most optimized vertical dynamic range for the HS Data burst.
4. Find the HS Data bursts. Depending on the number of HS Data burst configuration; if the current acquisition does not have enough HS Data burst, more acquisitions are required.
5. Collect all the required HS Data.
6. For the HS Data, common-mode waveform is required. The waveform can be constructed using the following equation:

   DataCommonMode = (Dp+Dn)/2
7. Apply an 8th-order Butterworth IIR bandpass filter, with a cutoff frequency of 450 MHz, to the common-mode waveform.
8. Measure the RMS voltage for the filtered waveform and record as $\Delta V_{CMTX(HF)}$.
9. Report the measurement results:
   - $\Delta V_{CMTX(HF)}$ value
10. Compare the measured $\Delta V_{CMTX(HF)}$ value with the conformance test limit.

Test References

See Table 17 - HS Transmitter AC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

HS Data Tx Common Level Variations Between 50-450 MHz Test Method of Implementation

The Common-Mode Voltage V_{CMTX} is defined as the arithmetic mean value of the voltages at the Dp and Dn pins. Because of various types of signal distortion that may occur, it is possible for V_{CMTX} to have different values when a Differential-1 vs. Differential-0 state is driven.

For this $\Delta V_{CMTX(LF)}$ test, the values for V_{CMTX} is obtained by using the following equation:

$$V_{CMTX} = \frac{V_{DP} + V_{DN}}{2}$$

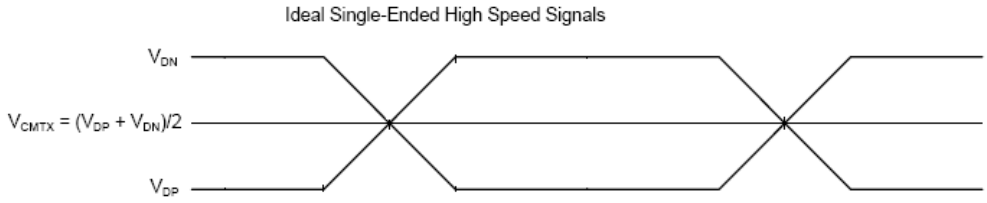

Figure 23 Ideal Single-Ended High Speed Signals

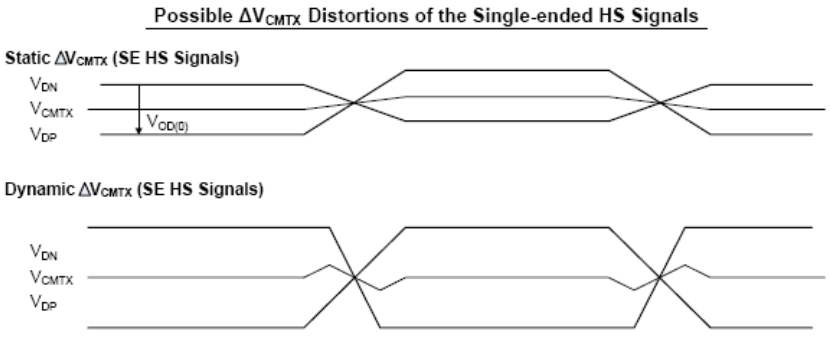

Figure 24 Possible Distortions of the ΔV_{CMTX} Single-Ended High Speed Signals

Test Definition Notes from the Specification

Table 18 HS Data Transmitter AC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMTX(LF)}$	Common level variation between 50-450 MHz			25	mV_{PEAK}	

PASS Condition

The measured $\Delta V_{CMTX(LF)}$ value for the test signal must be within the conformance limit as specified in Table 17 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Trigger at SoT of HS Data burst (LP11 to LP01).
2. Place the triggered edges on the left of the screen.
3. If Full HS Dynamic Range is configured, a pre-requisite step is executed to find the most optimized vertical dynamic range for HS Data burst.
4. Find the HS Data bursts. Depending on the number of HS Data burst configuration; if the current acquisition does not have enough HS Data burst, more acquisitions are required.
5. Collect all the required HS Data.
6. For the HS Data, common-mode waveform is required. The waveform can be constructed using the following equation:

   DataCommonMode = (Dp+Dn)/2
7. Apply an 8th-order Butterworth IIR bandpass filter, with –3dB cutoff frequencies of 50 and 450 MHz, to the common-mode waveform.
8. Measure the min and max voltage for the filtered waveform.
9. Select the worst absolute value for the min and max voltage and record it as $\Delta V_{CMTX(LF)}$.
10. Report the measurement results:
    - $\Delta V_{CMTX(LF)}$ value
11. Compare the measured $\Delta V_{CMTX(LF)}$ value with the conformance test limit.

Test References

See Table 17 - HS Transmitter AC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

HS Data Tx 20%-80% Rise Time Test Method of Implementation

The rise time, t_R is defined as the transition time between 20% and 80% of the full HS signal swing. The driver must meet the t_R specifications for all the allowable Z_{ID}.

Test Definition Notes from the Specification

Table 19 HS Data Transmitter AC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
t_R and t_F	20%-80% rise time and fall time			0.3	UI	1
		150			ps	

NOTE 1: UI is equal to 1/(2*fh).

The frequency 'fh' is the highest fundamental frequency for data transmission and is equal to $1/(2*UI_{INST,\ MIN})$. Implementers shall specify a value $UI_{INST,\ MIN}$ that represents the minimum instantaneous UI possible within a high speed data transfer for a given implementation.

PASS Condition

The measured t_R value for the test signal must be within the conformance limit as specified in Table 17 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. This test requires the following pre-requisite tests:
   - HS TX Differential Voltage (VOD)
   - actual VOD for Differential-1 and Differential-0 measurements are performed and test results are stored.
2. Trigger on SoT of HS Data burst (LP11->LP01).
3. Place the triggered edges on the left of the screen.
4. If Full HS Dynamic Range is configured, a pre-requisite step is executed to find out the most optimized vertical dynamic range for HS Data burst.
5. Find the HS Data bursts. Depending on the number of HS Data burst configuration, if the current acquisition does not have enough HS Data burst, more acquisitions are required.
6. Collect all the required HS Data.

7 Differential waveform is required. This can be achieved by taking the single-ended HS Data and form a differential waveform by using the following equation:

DataDiff = Dp-Dn

8 Define the measurement threshold as follows:

Top Level: V_{OD} for Differential-1

Base Level: V_{OD} for Differential-0

9 Measure all 20%-80% rise time at all the rising edges that meet the 20%-80% threshold criteria and record the values.

10 Report the measurement results.

a t_R (Max)

b t_R (Min)

c t_R (Mean)

11 Compare the measured t_R (Mean) value with the conformance test limit.

Test References

See Table 17 - HS Transmitter AC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

HS Data Tx 20%-80% Fall Time Test Method of Implementation

The rise time, t_F is defined as the transition time between 20% and 80% of the full HS signal swing. The driver must meet the t_F specifications for all the allowable Z_{ID}.

Test Definition Notes from the Specification

Table 20 HS Data Transmitter AC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
t_R and t_F	20%-80% rise time and fall time			0.3	UI	1
		150			ps	

NOTE 1: UI is equal to 1/(2*fh).

The frequency 'fh' is the highest fundamental frequency for data transmission and is equal to $1/(2*UI_{INST,\ MIN})$. Implementers shall specify a value $UI_{INST,\ MIN}$ that represents the minimum instantaneous UI possible within a high speed data transfer for a given implementation.

PASS Condition

The measured t_F value for the test signal must be within the conformance limit as specified in Table 17 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. This test requires the following pre-requisite tests:
   - HS TX Differential Voltage (VOD)
   - actual VOD for Differential-1 and Differential-0 measurements are performed and test results are stored.
2. Trigger on SoT of the HS Data burst (LP11->LP01).
3. Place the triggered edges on the left of the screen.
4. If Full HS Dynamic Range is configured, a pre-requisite step is executed to find out the most optimized vertical dynamic range for the HS Data burst.
5. Find the HS Data bursts. Depending on the number of HS Data burst configuration, if the current acquisition does not have enough HS Data burst, more acquisitions are required.
6. Collect all the required HS Data.

7 Differential waveform is required. This can be achieved by taking the single-ended HS Data and form a differential waveform by using the following equation:

DataDiff = Dp-Dn

8 Define the measurement threshold as follows:

Top Level: V_{OD} for Differential-1

Base Level: V_{OD} for Differential-0

9 Measure all 20%-80% fall time at all the falling edges that meet the 20%-80% threshold criteria and record the values.

10 Report the measurement results.

- **a** t_F (Max)
- **b** t_F (Min)
- **c** t_F (Mean)

11 Compare the measured t_F value with the conformance test limit.

Test References

See Table 17 - HS Transmitter AC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

4 Low Power Transmitter (LP Tx) Electrical Tests

This section provides the Methods of Implementation (MOIs) for the Low Power Transmitter (LP Tx) Electrical tests using an Agilent 80000, 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Conformance Test Application.

Probing for Low Power Transmitter Electrical Tests

When performing the LP Tx tests, the MIPI D-PHY Conformance Test Application will prompt you to make the proper connections. The connections for the LP Tx tests may look similar to the following diagram. Refer to the Connection tab in MIPI D-PHY Conformance Test Application for the exact number of probe connections.

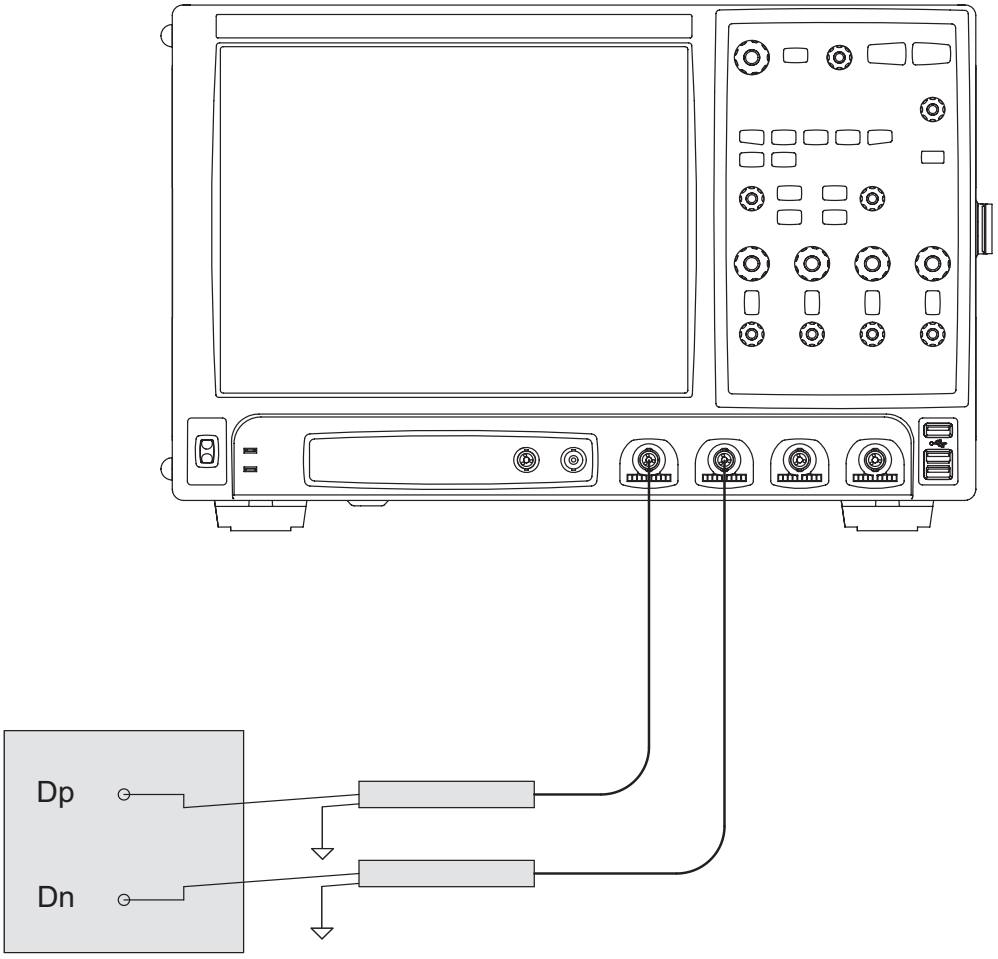

Figure 25 Probing for Low Power Transmitter Electrical Tests

You can identify the channels used for each signal in the Configuration tab of the MIPI D-PHY Conformance Test Application. (The channels shown in Figure 25 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 10, “InfiniiMax Probing,” starting on page 157.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Conformance Test Application" on page 21.

2 In the MIPI D-PHY Conformance Test application, click the Set Up tab.

3 Enter the High-Speed Data Rate, Device ID and User Comments.

4 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

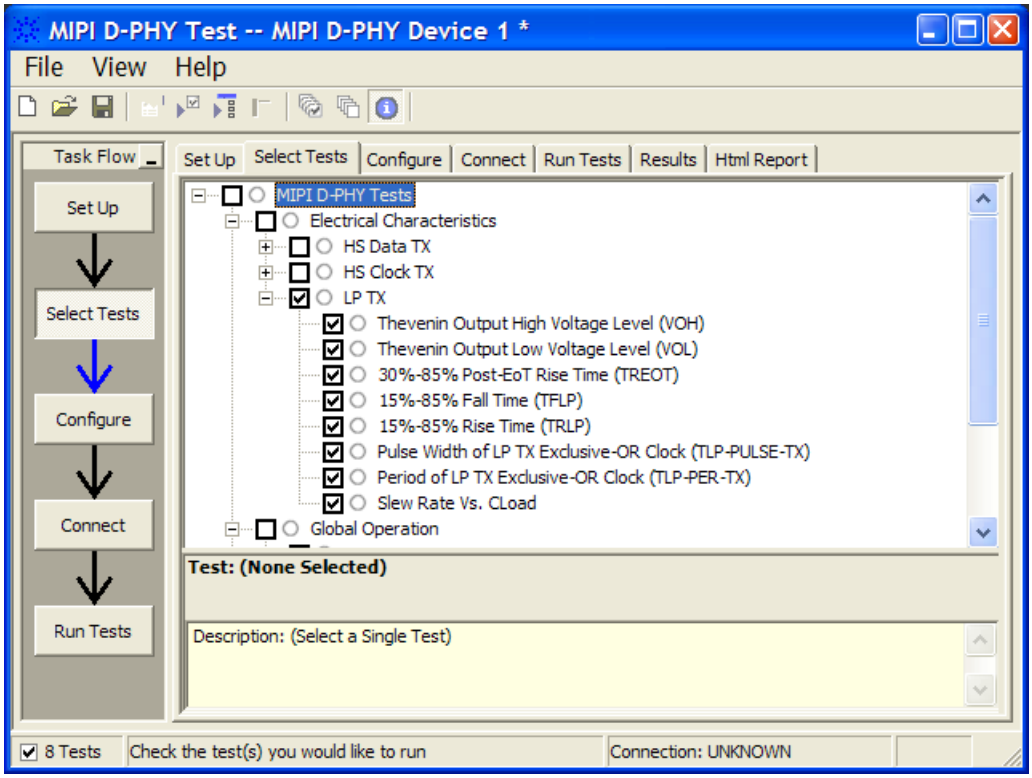

Figure 26 Selecting Low Power Transmitter Electrical Tests

5 Follow the MIPI D-PHY Conformance Test application's task flow to set up the configuration options (see Table 21), run the tests and view the tests results.

Table 21 Test Configuration Options

Configuration Option	Description
Scope Channel Resources	
Dp	Identifies the oscilloscope channels probing Dp signal.
Dn	Identifies the oscilloscope channels probing Dn signal.
CLK(Diff)	Identifies the oscilloscope channels probing clock (differentially).
CLKp	Identifies the oscilloscope channels probing clock.
CLKn	Identifies the oscilloscope channels probing clock.
Electrical Characteristics	
LP Tx	
LP Observations	Number of measurement instances to be observed.
LP Escape Timeout	Time in seconds the application waits before the LP Escape signal appears in each observation. Select 0 if the DUT is capable to output LP escape mode continuously. This option only affects LP tests that need LP Escape signal.
Measurement Time Range	Specifies the time range in nanoseconds the application uses when measuring DC and transition time of LP signal. Set it such that only one transition is visible during measurement.
Histogram Result	Select the histogram statistical result to be used in VOL and VOH tests.

LP Tx Thevein Output High Voltage Level Test Method of Implementation

The Low-Power transmitter is the slew-rate controlled push-pull driver. It is used for driving the lines in all low power operating modes. As such, it is important that the static power consumption of a LP transmitter be as low as possible. The slew-rate of signal transitions is bounded in order to keep the EMI (Electro Magnet Interface) low. V_{OH} is the Thevein output high-level voltage in the high-level state, when the pad pin is not loaded.

Test Definition Notes from the Specification

Table 22 LP Transmitter DC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
V_{OH}	Thevein output high level	1.1	1.2	1.3	V	

PASS Condition

The measured V_{OH} value for the test signal must be within the conformance limit as specified in Table 18 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Trigger the LP rising edge. Without the presence of LP Escape mode, the trigger still happens as the rising edge can be observed at EoT of HS Data burst.
2. Position the trigger point at the center of the screen and make sure that the stable LP high level voltage region is visible on the screen.
3. Accumulate the data by using the persistent display mode.
4. Turn on the histogram and take only the upper left of the screen.
5. Take the mode value of the histogram and use this value as V_{OH}.
6. Repeat the steps for Dn.
7. Report the measurement results.
   a. V_{OH} value for Dp channel
   b. V_{OH} value for Dn channel
8. Compare the measured V_{OH} worst value with the conformance test limit.

Test References

See Table 18 - LP Transmitter DC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

LP Tx Thevein Output Low Voltage Level Test Method of Implementation

V_{OL} is the Thevein output low-level voltage in the LP transmit mode. This is the voltage at an unloaded pad pin in the low level state.

Test Definition Notes from the Specification

Table 23 LP Transmitter DC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
V_{OL}	Thevein output low level	-50		50	mV	

PASS Condition

The measured V_{OH} value for the test signal must be within the conformance limit as specified in Table 18 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Trigger the LP falling edge. Without the presence of LP Escape mode, the trigger still happens as the falling edge can be observed at SoT of HS Data burst.
2. Position the trigger point at the center of the screen and make sure that the stable LP low level voltage region is visible on the screen.
3. Accumulate the data by using the persistent display mode.
4. Turn on the histogram and take only the lower left of the screen.
5. Take the mode value of the histogram and use this value as V_{OL} for Dp channel.
6. Repeat the steps for Dn.
7. Report the measurement results:
   a. V_{OL} value for Dp channel
   b. V_{OL} value for Dn channel
8. Compare the measured V_{OL} worst value with the conformance test limit.

Test References

See Table 18 - LP Transmitter DC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

LP Tx 15%-85% Rise Time Level Test Method of Implementation

The T_{RLP} is defined as 15%-85% rise time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD}. The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

Test Definition Notes from the Specification

Table 24 LP Transmitter AC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
T_{RLP} /T_{RLP}	15%-85% rise time and fall time			25	ns	1

NOTE 1: C_{LOAD} includes the low-frequency transmission line capacitance. The capacitance of Tx and Rx are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

PASS Condition

The measured T_{RLP} value for the test signal must be within the conformance limit as specified in Table 19 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. This test requires the following pre-requisite tests:
   a. LP Tx Thevenin Output High Voltage Level (V_{OH})
   b. LP Tx Thevenin Output Low Voltage Level (V_{OL})
   c. V_{OH} and V_{OL} values for Low Power signal measurements are performed and test results are stored.
2. All rising edge in LP are valid for this measurement except for EoT, thus the LP Escape mode is required for this test.
3. Setup the trigger on non-EoT LP rising-edges.
4. Depending on the number of observation configuration, the oscilloscope is triggered accordingly.
5. The average 15%-85% rise time for Dp is recorded.
6. Repeat the steps for Dn.
7. Report the measurement results:
   a. T_{RLP} value for Dp channel
   b. T_{RLP} value for Dn channel

8 Compare the measured T_{RLP} worst value with the conformance test limit.

Test References

See Table 19 - LP Transmitter AC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

LP Tx 15%-85% Fall Time Level Test Method of Implementation

The T_{FLP} is defined as 15%-85% fall time of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD}. The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages.

Test Definition Notes from the Specification

Table 25 LP Transmitter AC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
T_{RLP} /T_{RLP}	15%-85% rise time and fall time			25	ns	1

NOTE 1: C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of Tx and Rx are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

PASS Condition

The measured T_{FLP} value for the test signal must be within the conformance limit as specified in Table 19 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. This test requires the following pre-requisite tests:
   a. LP Tx Thevenin Output High Voltage Level (V_{OH})
   b. LP Tx Thevenin Output Low Voltage Level (V_{OL})
   c. V_{OH} and V_{OL} values for Low Power signal measurements are performed and test results are stored.
2. All falling edges in LP are valid for this measurement.
3. Setup the trigger on LP falling edges.
4. Depending on the number of observation configuration, the oscilloscope is triggered accordingly.
5. The average 15%-85% fall time for Dp is recorded.
6. Repeat the same trigger steps for Dn.
7. Report the measurement results:
   a. T_{FLP} average value for Dp channel
   b. T_{FLP} average value for Dn channel

8 Compare the measured T_{FLP} worst value with the conformance test limit.

Test References

See Table 19 - LP Transmitter AC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

LP Tx 30%-85% Post-EoT Rise Time Test Method of Implementation

The rise time of T_{REOT} starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to the stop of the differential drive.

Test Definition Notes from the Specification

Table 26 LP Transmitter AC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
T_{REOT}	30%-85% rise time and fall time			35	ns	1, 5, 6

NOTE 1: C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of Tx and Rx are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

NOTE 5: The rise time of T_{REOT} starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.

NOTE 6: With an addition load capacitance C_{CM} between 0-60pF on the termination centre tap at Rx side of the Lane.

PASS Condition

The measured T_{REOT} value for the test signal must be within the conformance limit as specified in Table 19 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. This test requires the following pre-requisite tests:
   - a LP Tx Thevenin Output High Voltage Level (V_{OH})
   - b LP Tx Thevenin Output Low Voltage Level (V_{OL})
   - c V_{OH} and V_{OL} values for Low Power signal measurements are performed and test results are stored.
2. Only LP rising edges during EoT are valid for this measurement.
3. Setup the trigger on LP rising edges during EoT.
4. Depending on the number of observation configuration, the oscilloscope is triggered accordingly.
5. The average 15%-85% rise time for Dp is recorded.

6 Repeat the same trigger steps for Dn.

7 Report the measurement results:

   a T_{REOT} average value for Dp channel

   b T_{REOT} average value for Dn channel

8 Compare the measured T_{REOT} worst value with the conformance test limit.

Test References

See Table 19 - LP Transmitter AC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

LP Tx Pulse Width of LP Tx Exclusive-Or Clock Test Method of Implementation

$T_{LP\text{-}PULSE\text{-}TX}$ is defined as the pulse width of the DUT Low-Power Tx XOR clock. A graphical representation of the XOR operation that creates the LP clock is shown below. The D-PHY Standard separates the $T_{LP\text{-}PULSE\text{-}TX}$ specification into two parts:

a The first LP XOR clock pulse after a Stop state, or the last LP XOR clock pulse before a Stop state must be wider than 40ns.

b All other LP XOR clock pulses must be wider than 20ns.

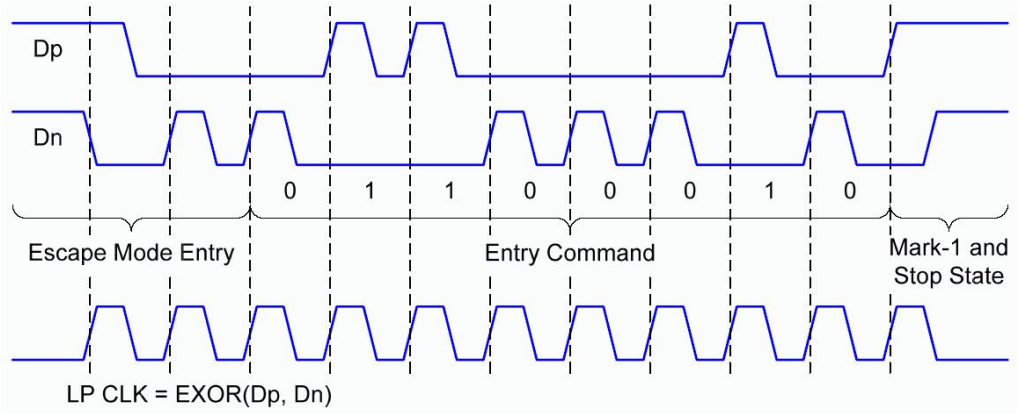

Figure 27 Graphical Representation of the XOR Operation

Test Definition Notes from the Specification

Table 27 LP Transmitter AC Specifications

Parameters	Description		Min	Nom	Max	Units	Notes
$T_{LP\text{-}PULSE\text{-}TX}$	Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40			ns	4
		All other pulses	20			ns	4

NOTE 4: This parameter value can be lower then T_{LPX} due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior.

PASS Condition

The measured $T_{LP\text{-}PULSE\text{-}TX}$ value for the test signal must be within the conformance limit as specified in Table 19 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Perform actual conformance testing (*CUSTLPXORClockAnalyzer*)
   a. Reset the oscilloscope
   b. Setup each channel for Dp and Dn to utilize the optimum vertical range
   c. Setup trigger condition on the oscilloscope based on LP trigger threshold value:
   - Use Advanced State Trigger Mode
   d. Check for a valid trigger occurrence
   e. Use *LocateMarkOneStop()* function to locate the Mark-1 and Stop State:
   - Define top/base values of Dn based on the measured VTOP and VBASE
   - Use 20%-50%-80% threshold definition for Dn
2. Generate the XOR clock waveform using FUNC1 and FUNC3 where $Clock_{XOR}$ = Abs [Dp-Dn].
3. Perform period and pulse width measurements on the generated XOR clock waveform function.
4. Report test results to the ATE framework:
   a. minimum XOR clock period
   b. minimum pulse width of XOR clock
5. Compare the measured minimum $T_{LP\text{-}PULSE\text{-}TX}$ value with the conformance test limit.

Test References

See Table 19 - LP Transmitter AC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

LP Tx Period of LP Tx Exclusive-Or Clock Test Method of Implementation

$T_{LP\text{-}PER\text{-}TX}$ is defined as the period of the DUT Low-Power Tx XOR clock. A graphical representation of the XOR operation that creates the LP clock is shown below. The D-PHY Standard separates the $T_{LP\text{-}PULSE\text{-}TX}$ specification into two parts:

a The first LP XOR clock pulse after a Stop state, or the last LP XOR clock pulse before a Stop state must be wider than 40ns.

b All other LP XOR clock pulses must be wider than 20ns.

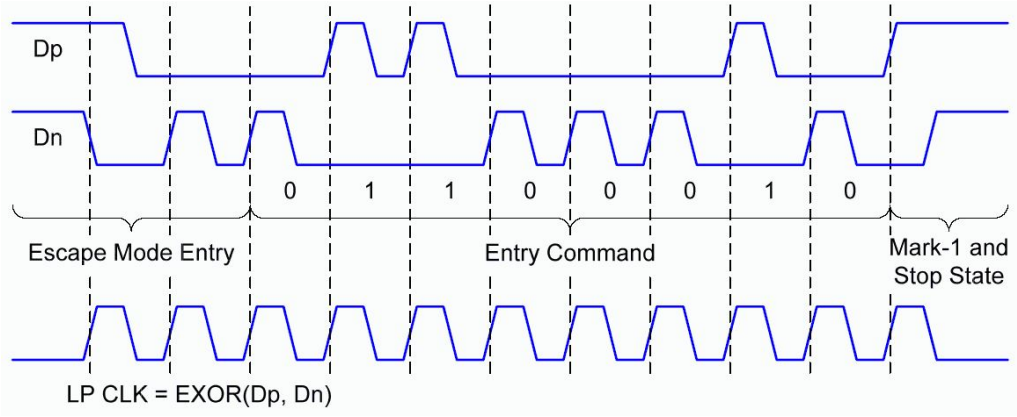

Figure 28 Graphical Representation of the XOR Operation

Test Definition Notes from the Specification

Table 28 LP Transmitter AC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
$T_{LP\text{-}PER\text{-}TX}$	Period of the LP exclusive-OR clock	90			ns	

PASS Condition

The measured $T_{LP\text{-}PER\text{-}TX}$ value for the test signal must be within the conformance limit as specified in Table 19 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1 Perform actual conformance testing (*CUSTLPXORClockAnalyzer*)

   a Translate the user input parameters (xml) from string to double

   b Reset the oscilloscope

   c Setup each channel for Dp and Dn to utilize the optimum vertical range

   d Setup trigger condition on the oscilloscope based on LP trigger threshold value

   Use Advanced State Trigger Mode

   e Check for a valid trigger occurrence

   f Use *LocateMarkOneStop()* function to locate the Mark-1 and Stop State

   Define top/base values of Dn based on the measured VTOP and VBASE

   Use 20%-50%-80% threshold definition for Dn

2 Generate the XOR clock waveform using FUNC1 and FUNC3 where $Clock_{XOR}$ = Abs [Dp-Dn].

3 Perform period and pulse width measurements on the generated XOR clock waveform function.

4 Report test results to the ATE framework:

   a minimum XOR clock period

   b minimum pulse width of XOR clock

5 Compare the measured minimum $T_{LP\text{-}PER\text{-}TX}$ value with the conformance test limit.

Test References

See Table 19 - LP Transmitter AC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

LP Tx Slew Rate vs C_{LOAD} Test Method of Implementation

The slew rate $\sigma V/\ \sigma t_{SR}$ is the derivative of the LP transmitter output signal voltage over time. The slew rate specification must be met for the 15%-85% range while driving a capacitive load, C_{LOAD}. The intention of specifying a maximum slew rate value in the specification is to limit the EMI (Electro Magnetic Interference).

The specification also states that the Slew Rate should be measured when the output voltage is between 15% and below 85% of the fully settled LP signal levels. This test value is also measured as an average across any 50mV segment of the output signal transition.

Test Definition Notes from the Specification

Table 29 LP Transmitter AC Specifications

Parameters	Description	Min	Nom	Max	Units	Notes
$\sigma V/\sigma t_{SR}$	Slew rate @ C_{LOAD} = 70pF	30		500	mV/ns	1, 2, 3, 7

NOTE 1: C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of Tx and Rx are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

NOTE 2: When the output voltage is between 15% and below 85% of the fully settled LP signal levels.

NOTE 3: Measured as average across any 50mV segment of the output signal transition.

NOTE 7: This value represents a corner point in a piece wise linear curve.

PASS Condition

The measured $\sigma V/\ \sigma t_{SR}$ value for the test signal must be within the conformance limit as specified in Table 19 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1 This test requires the following pre-requisite tests:

   a LP Tx Thevenin Output High Voltage Level (V_{OH})

   b LP Tx Thevenin Output Low Voltage Level (V_{OL})

   c V_{OH} and V_{OL} values for Low Power signal measurements are performed and test results are stored.

2 Perform actual conformance testing (*CUSTLPXORClockAnalyzer*)
   a Translate user input parameters (xml) from string to double.
   b Reset the oscilloscope and setup 2 grid displays; Grid1 for Dp and Grid2 for Dn signals.
   c Setup Dp and Dn channel to get the optimum vertical coverage.
3 Setup the triggering condition for 4 different conditions. On each condition, the slew rate measurement is performed on Dp or Dn:
   a LP rising edge on Dp signal. The results obtain would be Dp rising slew rates.
   b LP rising edge on Dn signal. The results obtain would be Dn rising slew rates.
   c LP falling edge on Dp signal. The results obtain would be Dp falling slew rates.
   d LP falling edge on Dn signal. The results obtain would be Dn falling slew rates.
4 Perform the slew rate measurement on Dp signal and store the max and min result value:
   a Find the 15% and 85% voltage point value based on the input V_{OH} and V_{OL}.
   b Find all the edges on Dp signal based on the 15% voltage point as the threshold level.
   c Find all the edges on Dp signal based on the 85% voltage point as the threshold level.
   d The slew rate is measured across any identified 50mV segment between the 15% and 85% point.
5 Report test results to the ATE framework:
   a minimum slew rate values for Dp and Dn signal.
   b maximum slew rate values for Dp and Dn signal.
6 Calculate the worst value of all the rising and falling slew rates for the Dp and Dn signals.

7 Report the measurement results.
   a Maximum slew rate value of Dp for rising edge.
   b Minimum slew rate value of Dp for rising edge.
   c Maximum slew rate value of Dn for rising edge.
   d Minimum slew rate value of Dn for rising edge.
   e Maximum slew rate value of Dp for falling edge.
   f Minimum slew rate value of Dp for falling edge.
   g Maximum slew rate value of Dn for falling edge.
   h Minimum slew rate value of Dn for falling edge.
8 Compare the measured worst slew rate value with the conformance test limit.

Test References

See Table 19 - LP Transmitter AC Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

Part II
Global Operation

Agilent Technologies

6 Data Transmitter (Data Tx) Global Operation Tests

This section provides the Methods of Implementation (MOIs) for the Data Transmitter (Data Tx) Global Operation tests using an Agilent 80000, 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Conformance Test Application.

Probing for Data Tx Global Operation Tests

When performing the Data Tx tests, the MIPI D-PHY Conformance Test Application will prompt you to make the proper connections. The connections for the Data Tx tests may look similar to the following diagram. Refer to the Connection tab in MIPI D-PHY Conformance Test Application for the exact number of probe connections.

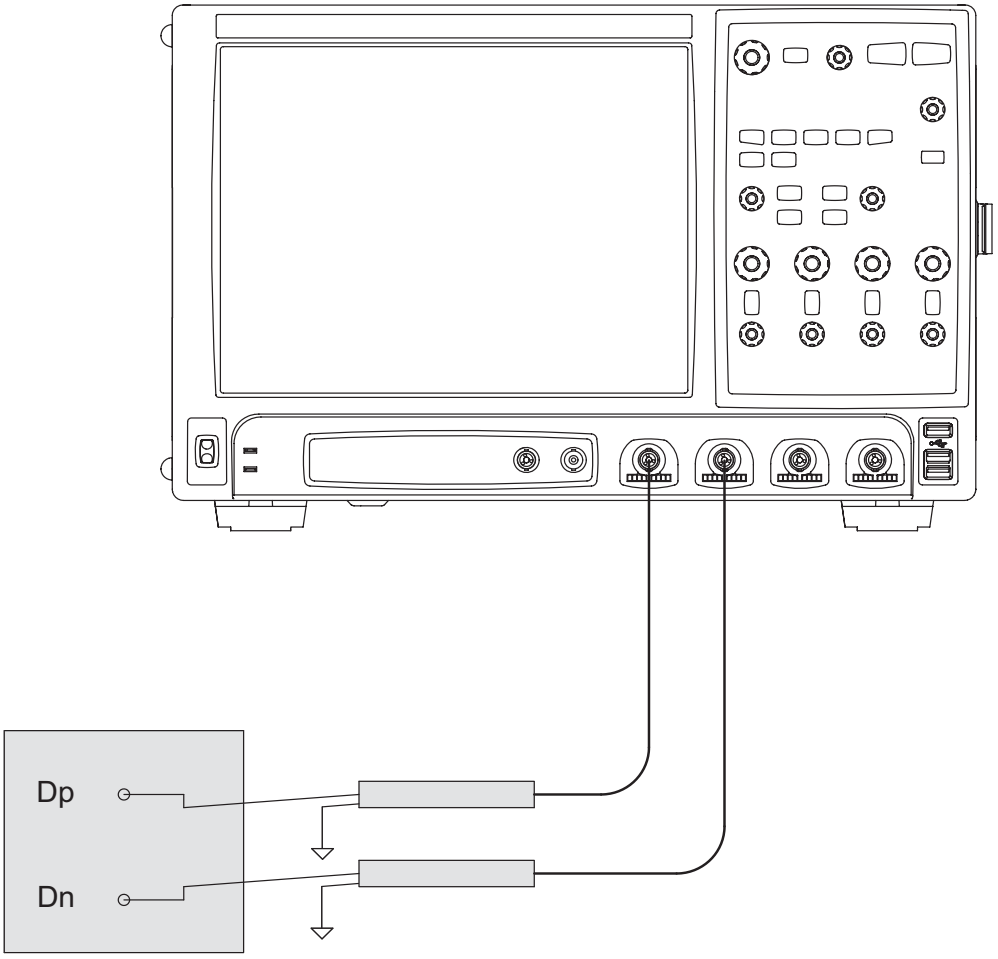

Figure 29 Probing for Data Tx Global Operation Tests

You can identify the channels used for each signal in the Configuration tab of the MIPI D-PHY Conformance Test Application. (The channels shown in Figure 29 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 10, “InfiniiMax Probing,” starting on page 157.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Conformance Test Application" on page 21.

2 In the MIPI D-PHY Conformance Test application, click the Set Up tab.

3 Enter the High-Speed Data Rate, Device ID and User Comments.

4 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

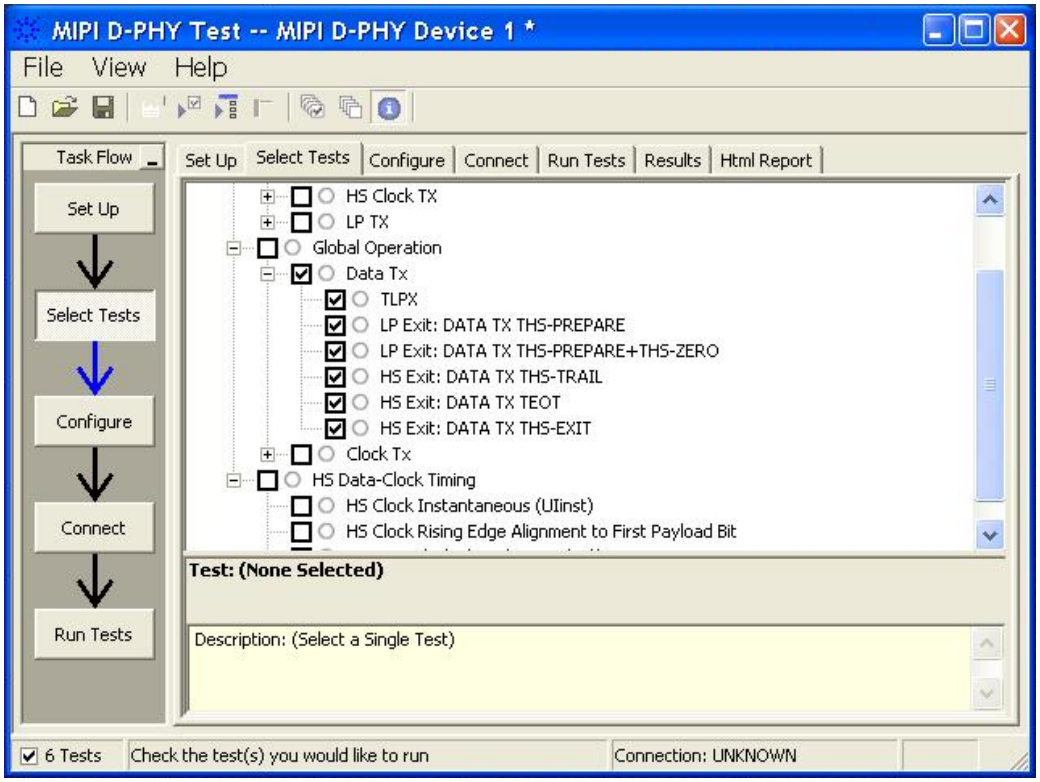

Figure 30 Selecting Data Tx Global Operation Tests

5 Follow the MIPI D-PHY Conformance Test application's task flow to set up the configuration options (see Table 30), run the tests and view the tests results.

Table 30 Test Configuration Options

Configuration Option	Description
Scope Channel Resources	
Dp	Identifies the oscilloscope channels probing Dp signal.
Dn	Identifies the oscilloscope channels probing Dn signal.
CLK(Diff)	Identifies the oscilloscope channels probing clock (differentially).
CLKp	Identifies the oscilloscope channels probing clock.
CLKn	Identifies the oscilloscope channels probing clock.
Global Operation	
Number of HS burst	Number of HS burst to be observed in Data and Clock tests. For Clock, if Clock signal doesn't contain LP signal, 2M sample points will be used instead.
VIL (max)	VIL(max) is used to determine the starting point of the TLPX and THS-PREPARE. Please see D-Phy specification 0.9 section 8.2.2 Table 22 for the allowable value.
VIH (min)	VIH(min) is used to determine the ending point of the CLK TX TEOT. Please see D-Phy specification 0.9 section 8.2.2 Table 22 for the allowable value.
VIDTH (max)	VIDTH(max) is used to determine the stop point of the THS-PREPARE. Please see D-Phy specification 0.9 section 8.2.1 Table 20 for the allowable value.

TLPX Test Method of Implementation

This test verifies that the last LP-01's duration prior to HS Data burst is within the specification.

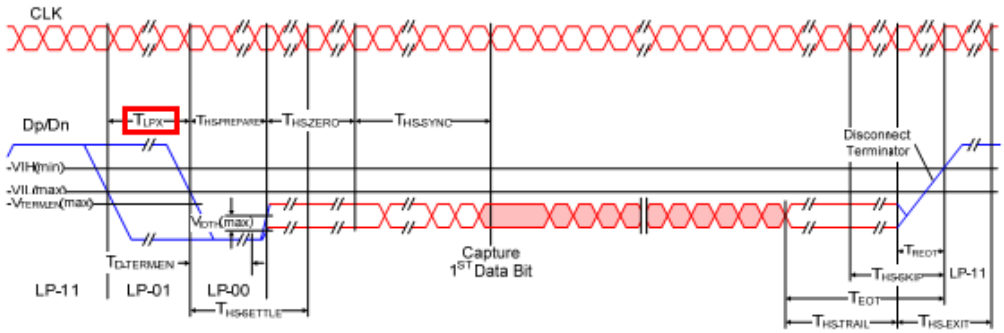

Figure 31 High-Speed Data Transmission in Bursts

Test Definition Notes from the Specification

Table 31 Global Operation Timing Parameters

Parameters	Description	Min	Typ	Max	Units	Notes
T_{LPX}	Length of any Low-Power state period	50			ns	4

NOTE 4: T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

PASS Condition

The average T_{LPX} must be within the conformance limit as specified in Table 14 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Trigger on the Dp's falling edge in LP-01 at the SoT.
2. Denote the time when the Dp falling edge first crosses VIL(max), as T1.
3. Denote the time when the first Dn falling edge after T1 crosses VIL(max), as T2.
4. Calculate T_{LPX} by using the following equation:

   T_{LPX} = T2-T1
5. Repeat step 1 to step 4 for a required number of observations.

6 Report the average T_{LPX}.

7 Compare the average T_{LPX} value with the conformance test limit.

Test References

See Table 14 - Global Operation Timing Parameters, in the *MIPI Alliance Standard for D-PHY v0.9*.

LP Exit: Data Tx THS-PREPARE Test Method of Implementation

This test verifies that the last LP-00's duration prior to HS Data burst is within the specification.

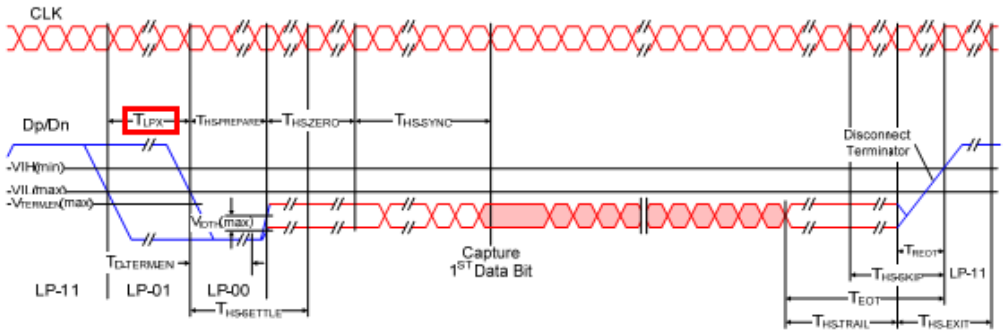

Figure 32 High-Speed Data Transmission in Bursts

Test Definition Notes from the Specification

Table 32 Global Operation Timing Parameters

Parameters	Description	Min	Typ	Max	Units	Notes
$T_{HS\text{-}PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40 ns+4*UI		85 ns + 6 * UI	ns	

PASS Condition

The average $T_{HS\text{-}PREPARE}$ must be within the conformance limit as specified in Table 14 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Trigger on the Dp's falling edge in LP-01 at the SoT.
2. Denote the time when the first Dn falling edge after LP-01 crosses VIL(max), as T2.
3. Construct the differential waveform of Dp and Dn by using the following formula:

   DataDiff = Dp-Dn

4. Find and denote the first falling edge of the differential waveform that crosses - V_{IDTH}(max) as T3. T3 must be > T2.
5. Calculate $T_{HS\text{-}PREPARE}$ by using the following equation:

   $T_{HS\text{-}PREPARE}$ = T3-T2

6 Repeat step 1 to step 5 for a required number of observations.

7 Report the average $T_{HS-PREPARE}$.

8 Compare the average $T_{HS-PREPARE}$ value with the conformance test limit.

Test References

See Table 14 - Global Operation Timing Parameters, in the *MIPI Alliance Standard for D-PHY v0.9*.

LP Exit: Data Tx THS-PREPARE + THS-ZERO Test Method of Implementation

This test verifies that the duration of HS Tx driving the line in HS0 prior to HS Sync sequence is within the specification. HS Sync-Sequence: 0001110101.

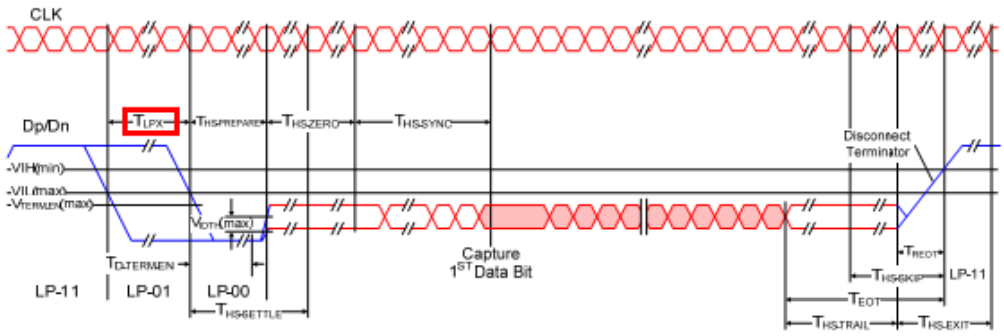

Figure 33 High-Speed Data Transmission in Bursts

Test Definition Notes from the Specification

Table 33 LP Transmitter AC Specifications

Parameters	Description	Min	Typ	Max	Units	Notes
$T_{HS\text{-}PREPARE} + T_{HS\text{-}ZERO}$	$T_{HS\text{-}PREPARE}$ + Time to drive HS-0 before the Sync sequence	145 ns+10*IU			ns	

PASS Condition

The average $T_{HS\text{-}PREPARE} + T_{HS\text{-}ZERO}$ must be within the conformance limit as specified in Table 14 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Trigger on Dp's falling edge in LP-01 at the SoT.
2. Denote the time when the first Dn falling edge after Dp falling crosses VIL(max), as T2.
3. Construct the differential waveform of Dp and Dn by using the following formula:

   DataDiff = Dp-Dn

4. Find and denote the first rising edge of the differential waveform that crosses $-V_{IDTH}$(max) as T4. T4 must be > T2 and > T3.

5 T4 is where 000 in HS Sync sequence ends.

6 Find and denote the next rising edge that crosses V_{IDTH}(max) after T4 as T5.

7 T5 is where 111 in HS Sync sequence ends.

8 The 000 of HS Sync sequence should be the same length in time as the 111, thus the time duration for 000 should be T5 - T4.

9 Calculate $T_{HS\text{-}PREPARE} + T_{HS\text{-}ZERO}$ by using the following equation:

$$T_{HS\text{-}PREPARE} + T_{HS\text{-}ZERO} = T4\text{-}(T5\text{-}T4)\text{-}T2$$

10 Repeat step 1 to step 4 for a required number of observations.

11 Report the average $T_{HS\text{-}PREPARE} + T_{HS\text{-}ZERO}$.

12 Compare the average $T_{HS\text{-}PREPARE} + T_{HS\text{-}ZERO}$ with the conformance test limit.

Test References

See Table 14 - Global Operation Timing Parameters, in the *MIPI Alliance Standard for D-PHY v0.9*.

HS Exit: Data TX THS-TRAIL Test Method of Implementation

This test verifies that the duration of HS Tx driving the line in inverted final differential state following the last payload data bit of a HS Data burst is equal or greater than the minimum required value.

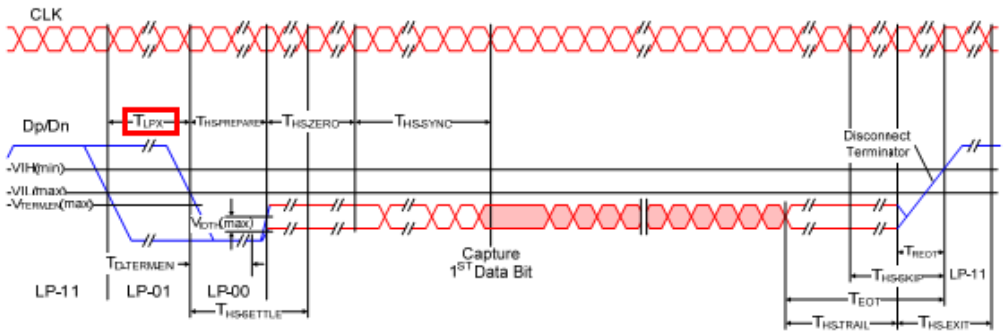

Figure 34 High-Speed Data Transmission in Bursts

Test Definition Notes from the Specification

Table 34 Global Operation Timing Parameters

Parameters	Description	Min	Typ	Max	Units	Notes
$T_{HS\text{-}TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (n*8*UI, 60 ns+n*4*UI)			ns	2,3

NOTE 2: If a > b the max(a,b) = a otherwise max(a,b) = b.

NOTE 3: Where n = 1 for Forward-direction HS mode and n = 4 for Reverse-direction HS mode.

PASS Condition

The average $T_{HS\text{-}TRAIL}$ must be equal or greater than the conformance limit as specified in Table 14 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Trigger on Dp's falling edge in LP-01 at the SoT.
2. Go to EoT of the same burst.
3. Find the time when the last payload data bit's differential edge crosses +/-V_{IDTH}(max), denoted as T6.

4 Find the time when the last Tx differential edge crosses +/-V_{IDTH}(max), and denote it as T7. Note that T7 must be greater than T6.

5 Use the following calculation:

$T_{HS\text{-}TRAIL}$ = T7-T6.

6 Repeat step 1 to step 5 for a required number of observations.

7 Report the average $T_{HS\text{-}TRAIL}$.

8 Compare the average $T_{HS\text{-}TRAIL}$ with the conformance test limits.

Test References

See Table 14 - Global Operation Parameters Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

HS Exit: Data Tx TEOT Test Method of Implementation

This test verifies that the combined duration of the $T_{HS\text{-}TRAIL}$ and T_{REOT} intervals of the DUT Data Tx is less than the maximum required value.

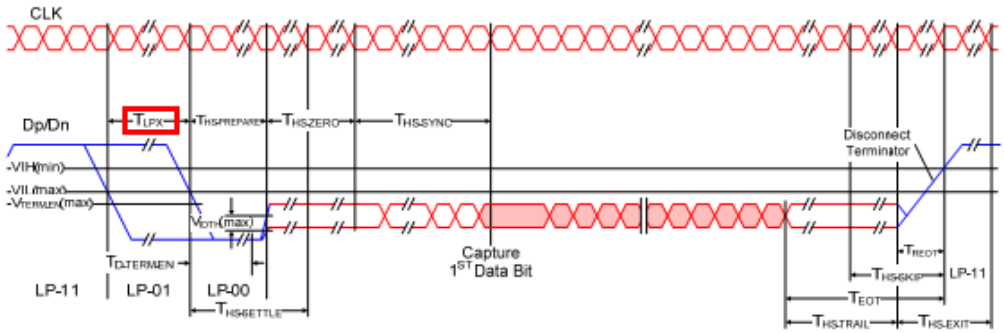

Figure 35 High-Speed Data Transmission in Bursts

Test Definition Notes from the Specification

Table 35 Global Operation Timing Parameters

Parameters	Description	Min	Typ	Max	Units	Notes
T_{EOT}	Time from start of $T_{HS\text{-}TRAIL}$ or $T_{CLK\text{-}TRAIL}$ period to start of LP-11 state			105 ns+n*12*UI	ns	3

NOTE 3: Where n = 1 for Forward-direction HS mode and n = 4 for Reverse-direction HS mode.

PASS Condition

The average T_{EOT} value must be equal or less than the conformance limit as specified in Table 14 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Trigger on Dp's falling edge in LP-01 at the SoT.
2. Go to EoT.
3. Find the time when the last data differential edge crosses +/-V_{IDTH}(max), and denote it as T6.
4. Find the time where Dp rising edge crosses VIH(min), and denote it as T8. Note that T8 must greater than T6.

5 Use the following calculation:

T_{EOT} = T8-T6.

6 Repeat step 1 to step 5 for a required number of observations.

7 Report the average T_{EOT}.

8 Compare the average T_{EOT} with the conformance test limits.

Test References

See Table 14 - Global Operation Timing Parameters, in the *MIPI Alliance Standard for D-PHY v0.9*.

HS Exit: Data Tx THS-EXIT Test Method of Implementation

This test verifies that the Data Tx remains in LP-11 state after exiting HS mode is greater than the minimum required value.

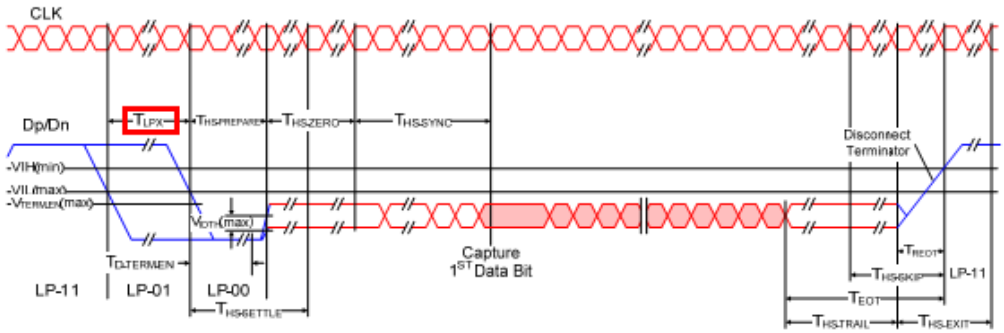

Figure 36 High-Speed Data Transmission in Bursts

Test Definition Notes from the Specification

Table 36 Global Operation Timing Parameters

Parameters	Description	Min	Typ	Max	Units	Notes
$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100			ns	

PASS Condition

The average $T_{HS-EXIT}$ value must be equal or greater than the conformance limit as specified in Table 14 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Trigger on the Dp's falling edge in LP-01 at the SoT.
2. Go to EoT of the same burst.
3. Find the time when the last Data Tx differential edge crosses +/-V_{IDTH}(max), and denote it as T7.
4. Find the time after T7 when Dp falling edge starts to cross VIL(min), and denote it as T9.
5. Use the following calculation:

   $T_{HS-EXIT}$ = T9-T7.
6. Repeat step 1 to step 5 for a required number of observations.

7 Report the average $T_{HS-EXIT}$.

8 Compare the average $T_{HS-EXIT}$ with the conformance test limits.

Test References

See Table 14 - Global Operation Timing Parameters, in the *MIPI Alliance Standard for D-PHY v0.9*.

7 Clock Transmitter (Clock Tx) Global Operation Tests

This section provides the Methods of Implementation (MOIs) for the Clock Transmitter (Clock Tx) Global Operation tests using an Agilent 80000, 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Conformance Test Application.

Probing for Clock Tx Global Operation Tests

When performing the Clock Tx tests, the MIPI D-PHY Conformance Test Application will prompt you to make the proper connections. The connections for the Clock Tx tests may look similar to the following diagram. Refer to the Connection tab in MIPI D-PHY Conformance Test Application for the exact number of probe connections.

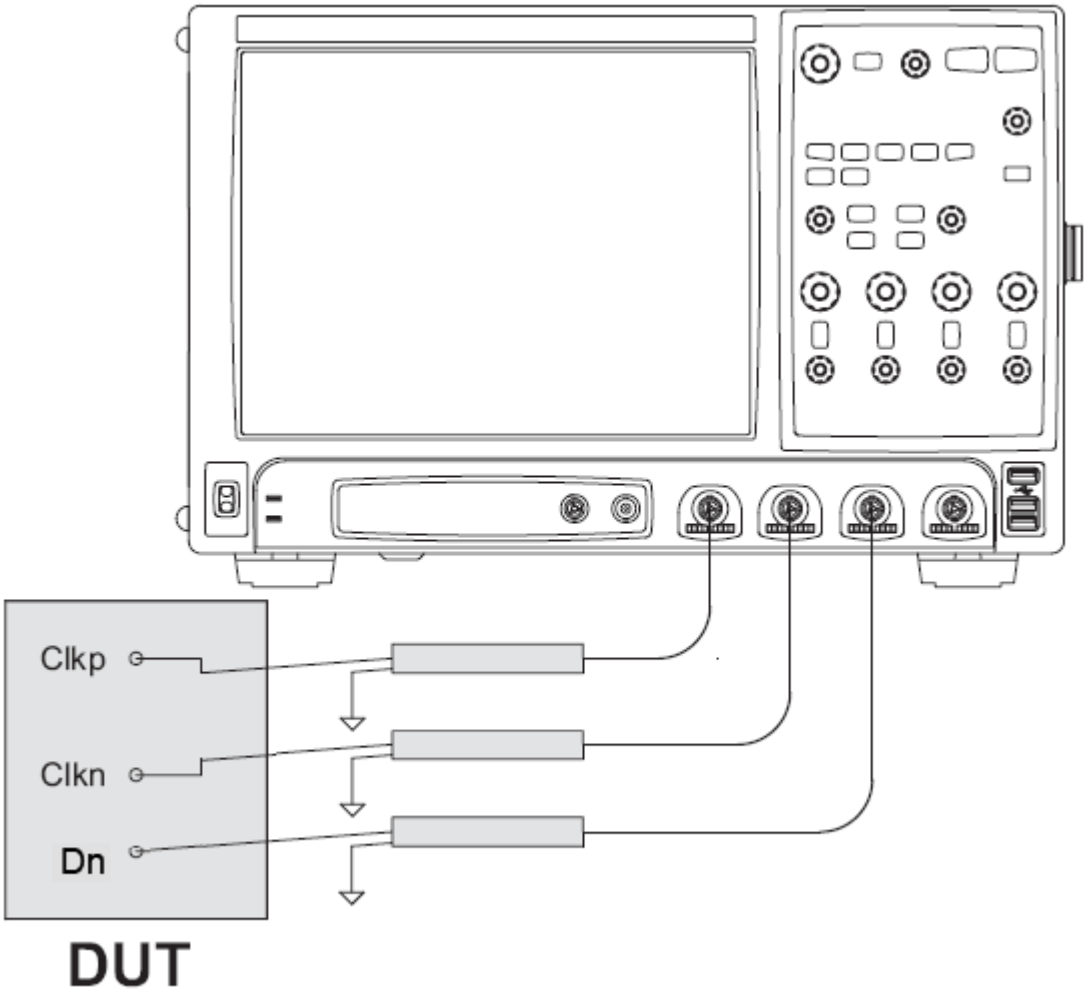

Figure 37 Probing for Clock Tx Global Operation Tests

You can identify the channels used for each signal in the Configuration tab of the MIPI D-PHY Conformance Test Application. (The channels shown in Figure 37 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 10, “InfiniiMax Probing,” starting on page 157.

Test Procedure

1 Start the automated test application as described in "Starting the MIPI D-PHY Conformance Test Application" on page 21.

2 In the MIPI D-PHY Conformance Test application, click the Set Up tab.

3 Enter the High-Speed Data Rate, Device ID and User Comments.

4 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

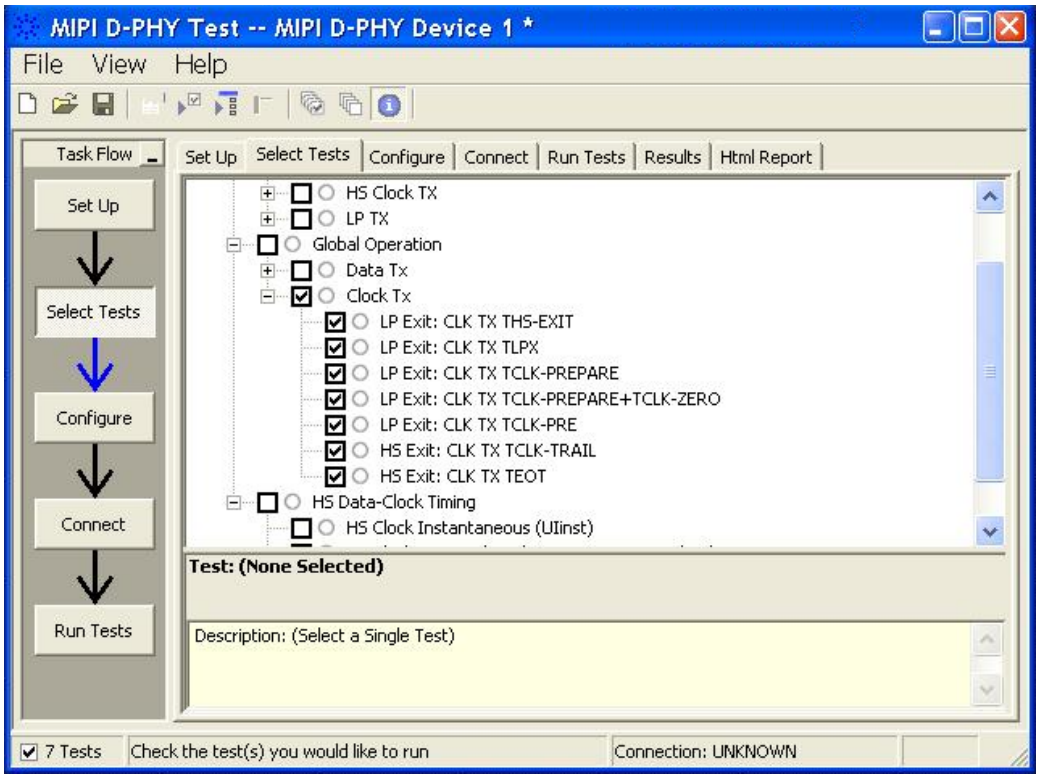

Figure 38 Selecting Clock Tx Global Operation Tests

5 Follow the MIPI D-PHY Conformance Test application's task flow to set up the configuration options (see Table 37), run the tests and view the tests results.

Table 37 Test Configuration Options

Configuration Option	Description
Scope Channel Resources	
Dp	Identifies the oscilloscope channels probing Dp signal.
Dn	Identifies the oscilloscope channels probing Dn signal.
CLK(Diff)	Identifies the oscilloscope channels probing clock (differentially).
CLKp	Identifies the oscilloscope channels probing clock.
CLKn	Identifies the oscilloscope channels probing clock.
Global Operation	
Number of HS burst	Number of HS burst to be observed in Data and Clock tests. For Clock, if Clock signal doesn't contain LP signal, 2M sample points will be used instead.
VIL (max)	VIL(max) is used to determine the starting point of the TLPX and THS-PREPARE. Please see D-Phy specification 0.9 section 8.2.2 Table 22 for the allowable value.
VIH (min)	VIH(min) is used to determine the ending point of the CLK TX TEOT. Please see D-Phy specification 0.9 section 8.2.2 Table 22 for the allowable value.
VIDTH (max)	VIDTH(max) is used to determine the stop point of the THS-PREPARE. Please see D-Phy specification 0.9 section 8.2.1 Table 20 for the allowable value.

LP Exit: CLK Tx THS-EXIT Test Method of Implementation

This test verifies that the duration for the Clock Tx to remain in LP-11 (Stop) state after exiting the HS mode is greater than the minimum required value.

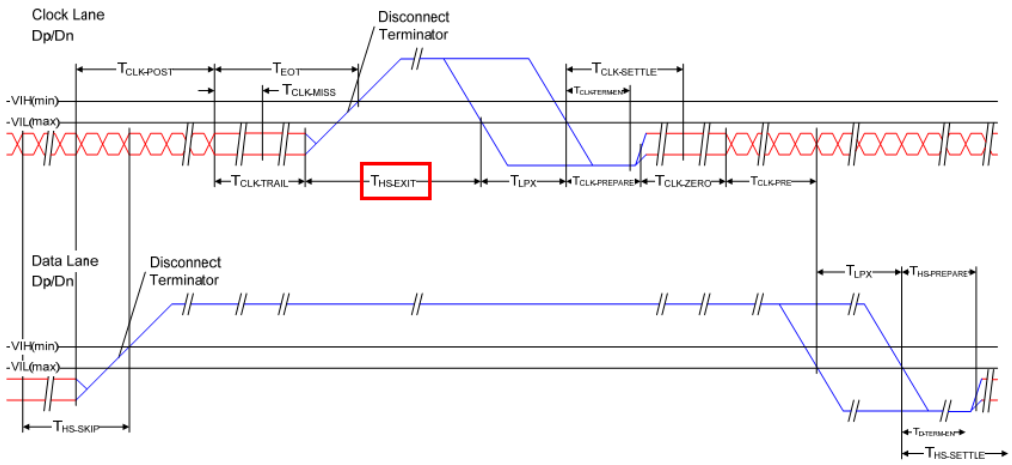

Figure 39 Switching the Clock Lane between Clock Transmission and Low-Power Mode

Test Definition Notes from the Specification

Table 38 Global Operation Timing Parameters

Parameters	Description	Min	Typ	Max	Units	Notes
$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100			ns	

PASS Condition

The average $T_{HS-EXIT}$ must be within the conformance limit as specified in Table 14 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Trigger on the Clkn's falling edge after LP-01.
2. Find the time when the Clkp falling edge (that happens before the trigger position) crosses VIL(max) and denote it as T1.
3. Construct the differential clock waveform by using the following equation:

   DiffClock = Clkp-Clkn

4 Find the time when DiffClock last crosses $+V_{IDTH}(max)$ or $-V_{IDTH}(max)$ before T1, denote it as T0.

5 Calculate $T_{HS-EXIT}$ by using the following equation:

$$T_{HS-EXIT} = T1-T0$$

6 Repeat step 1 to step 5 for a required number of observations.

7 Report the average $T_{HS-EXIT}$.

8 Compare the average $T_{HS-EXIT}$ value with the conformance test limit.

Test References

See Table 14 - Global Operation Timing Parameters, in the *MIPI Alliance Standard for D-PHY v0.9*.

LP Exit: CLK Tx TLPX Test Method of Implementation

This test verifies that the duration for the Clock Tx to remain in LP-01 (Stop) before entering HS mode is greater than the minimum required value.

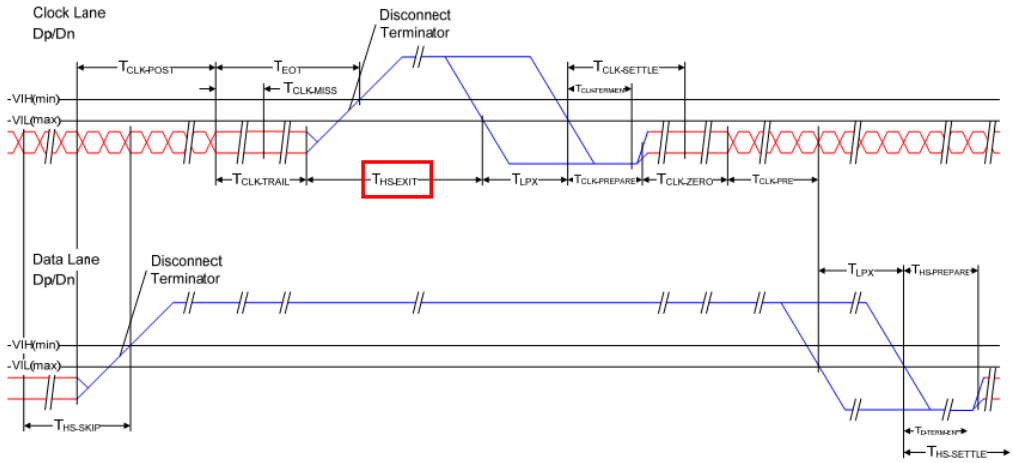

Figure 40 Switching the Clock Lane between Clock Transmission and Low-Power Mode

Test Definition Notes from the Specification

Table 39 Global Operation Timing Parameters

Parameters	Description	Min	Typ	Max	Units	Notes
T_{LPX}	Length of any Low-Power state period	50			ns	4

NOTE 4: T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

PASS Condition

The average T_{LPX} must be within the conformance limit as specified in Table 14 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Trigger on the Clkn's falling edge in LP-01.
2. Find the time when the Clkp's falling edge (that happens before the trigger position) crosses VIL(max) and denote it as T1.
3. Find the time when the Clkn's falling edge (that happens after T1) crosses VIL(max) and denote it as T2.

4 Calculate T_{LPX} by using the following equation:

$$T_{LPX} = T2\text{-}T1$$

5 Repeat step 1 to step 4 for a required number of observations.

6 Report the average T_{LPX}.

7 Compare the average T_{LPX} value with the conformance test limit.

Test References

See Table 14 - Global Operation Timing Parameters, in the *MIPI Alliance Standard for D-PHY v0.9*.

LP Exit: CLK Tx TCLK-PREPARE Test Method of Implementation

This test verifies that the duration of Clock Tx to remain in LP-00 state before entering HS mode is within the required value.

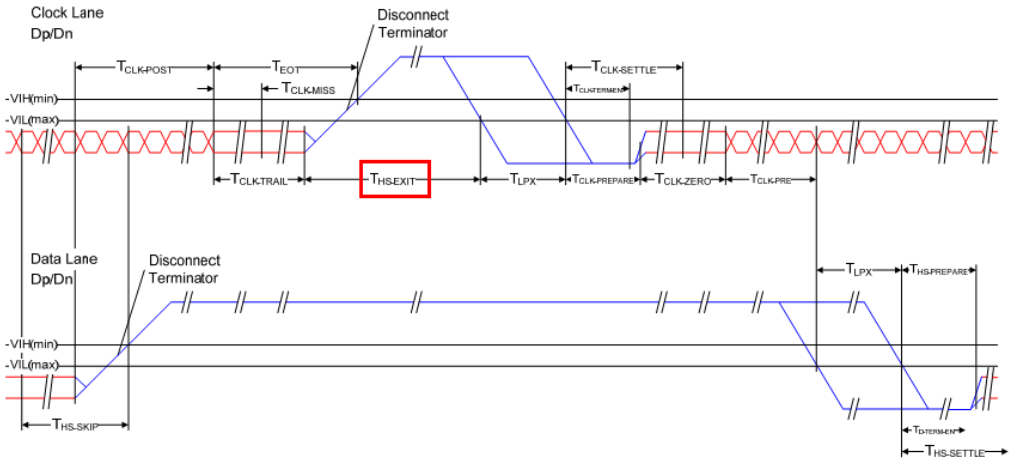

Figure 41 Switching the Clock Lane between Clock Transmission and Low Power Mode

Test Definition Notes from the Specification

Table 40 Global Operation Timing Parameters

Parameters	Description	Min	Typ	Max	Units	Notes
$T_{CLK\text{-}PREPARE}$	Time to drive LP-00 to prepare for HS clock transmission	38		95	ns	

PASS Condition

The average $T_{CLK\text{-}PREPARE}$ must be within the conformance limit as specified in Table 14 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Trigger on the Clkn's falling edge in LP-01.
2. Find the time when the Clkp's falling edge (that happens before the trigger position) crosses V_{IL}(max) and denote it as T1.
3. Find the time when the Clkn's falling edge (that happens after T1) crosses V_{IL}(max) and denote it as T2.
4. Construct the differential clock waveform by using the following equation:

DiffClock = Clkp- Clkn

5 Find the time when the DiffClock's falling edge first crosses $-V_{IDTH}$(max) and denote it as T3.

6 Calculate $T_{CLK-PREPARE}$ by using the following equation:

$T_{CLK-PREPARE}$ = T3-T2

7 Repeat step 1 to step 6 for a required number of observations.

8 Report the average $T_{CLK-PREPARE}$.

9 Compare the average $T_{CLK-PREPARE}$ value with the conformance test limit.

Test References

See Table 14 - Global Operation Timing Parameters, in the *MIPI Alliance Standard for D-PHY v0.9*.

LP Exit: CLK Tx TCLK-PREPARE + TCLK-ZERODATA Test Method of Implementation

This test verifies that the duration or the Clock Tx to remain in LP-00 and HS0 state before starting clock transmission is greater than the minimum required value.

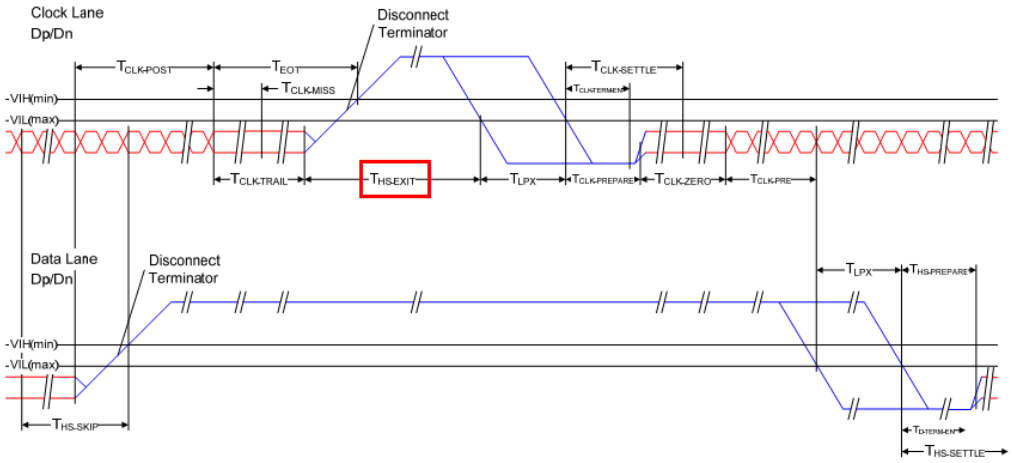

Figure 42 Switching the Clock Lane Between Clock Transmission and Low-Power Mode

Test Definition Notes from the Specification

Table 41 Global Operation Timing Parameters

Parameters	Description	Min	Typ	Max	Units	Notes
$T_{CLK\text{-}PREPARE}$+$T_{CLK\text{-}ZERO}$	$T_{CLK\text{-}PREPARE}$ + time for lead HS-0 drive period before starting Clock	300			ns	

PASS Condition

The average $T_{CLK\text{-}PREPARE}$ + $T_{CLK\text{-}ZERO}$ must be within the conformance limit as specified in Table 14 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Trigger on the Clkn's falling edge in LP-01.
2. Find the time when the Clkp's falling edge (that happens before the trigger position) crosses V_{IL}(max) and denote it as T1.
3. Find the time when the Clkn's falling edge (that happens after T1) crosses V_{IL}(max) and denote it as T2.

4 Construct the differential clock waveform by using the following equation:

$$DiffClock = Clkp - Clkn$$

5 Find the time when the DiffClock's falling edge first crosses $-V_{IDTH}(max)$ after T2 and denote it as T3.

6 Find the time when the DiffClock's rising edge first crosses $-V_{IDTH}(max)$ after T3 and denote it as T4.

7 Calculate $T_{CLK-PREPARE} + T_{CLK-ZERO}$ by using the following equation:

$$T_{CLK-PREPARE} + T_{CLK-ZERO} = T4 - T2$$

8 Repeat step 1 to step 7 for a required number of observations.

9 Report the average $T_{CLK-PREPARE} + T_{CLK-ZERO}$.

10 Compare the average $T_{CLK-PREPARE} + T_{CLK-ZERO}$ value with the conformance test limit.

Test References

See Table 14 - Global Operation Parameters Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

LP Exit: CLK Tx TCLK-PRE Test Method of Implementation

This test verifies that the combined duration of the $T_{HS\text{-}TRAIL}$ and T_{REOT} intervals of the DUT Data Tx is less than the maximum required value.

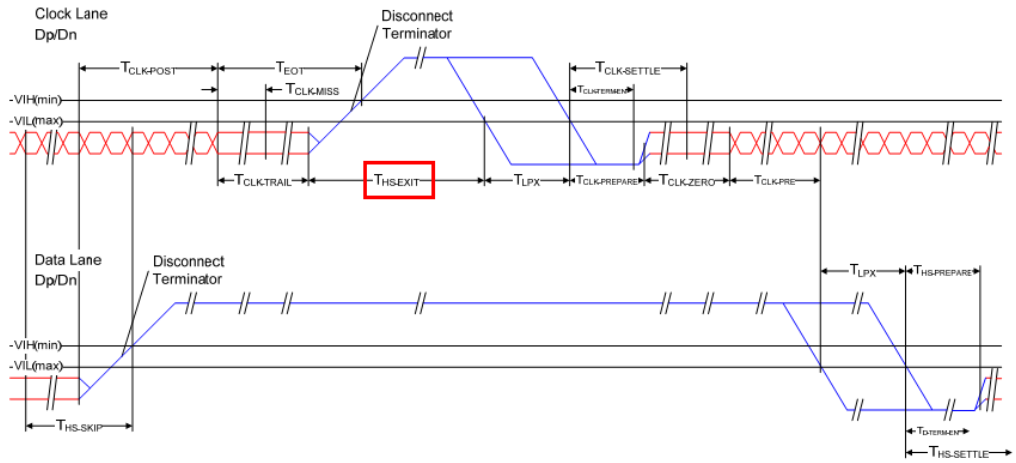

Figure 43 Switching the Clock Lane Between Clock Transmission and Low-Power Mode

Test Definition Notes from the Specification

Table 42 Global Operation Timing Parameters

Parameters	Description	Min	Typ	Max	Units	Notes
$T_{CLK\text{-}PRE}$*	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI	

*

PASS Condition

The average $T_{CLK\text{-}PRE}$ value must be within the conformance limit as specified in Table 14 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1 Trigger on the Clkn's falling edge in LP-01.

2 Construct the differential clock waveform by using the following equation:

DiffClock = Clkp-Clkn

3 Find the time when the DiffClock's rising edge first crosses $-V_{IDTH}(max)$ after LP-00 and denote it as T4.

4 Find the time when the Dp's LP falling edge first crosses V_{IL}(max) after and denote it as T5.

5 Calculate $T_{CLK\text{-}PRE}$ by using the following equation:

$$T_{CLK\text{-}PRE} = T5\text{-}T4$$

6 Repeat step 1 to step 5 for a required number of observations.

7 Report the average $T_{CLK\text{-}PRE}$.

8 Compare the average $T_{CLK\text{-}PRE}$ value with the conformance test limit.

Test References

See Table 14 - Global Operation Timing Parameters, in the *MIPI Alliance Standard for D-PHY v0.9*.

LP Exit: CLK Tx TCLK-TRAIL Test Method of Implementation

This test verifies the duration for Clock Tx to drive the final HS-0 differential state following the last payload clock bit, is equal or greater than the minimum required value.

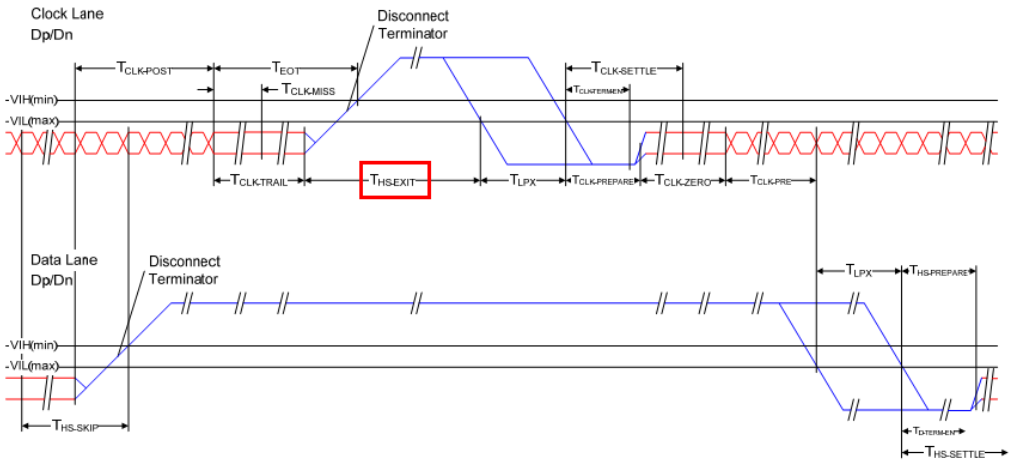

Figure 44 Switching the Clock Lane Between Clock Transmission and Low-Power Mode

Test Definition Notes from the Specification

Table 43 Global Operation Timing Parameters

Parameters	Description	Min	Typ	Max	Units	Notes
$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60			ns	

PASS Condition

The average $T_{CLK-TRAIL}$ must be equal or greater than the conformance limit as specified in Table 14 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Trigger on the Clkn's falling edge in LP-01.
2. Back trace to the previous EoT.
3. Construct the differential clock waveform by using the following equation:

   DiffClock = Clkp-Clkn

4 Find the time when the DiffClock crosses +/-V_{IDTH}(max) after last payload clock bit and denote it as T6.

5 Find the time when the DiffClock crosses +/-V_{IDTH}(max) before switching to LP. Denote the time as T7. Note that T7 must be greater than T6.

6 Calculate $T_{CLK\text{-}TRAIL}$ by using the following equation:

$$T_{CLK\text{-}TRAIL} = T7\text{-}T6$$

7 Repeat step 1 to step 6 for a required number of observations.

8 Report the average $T_{CLK\text{-}TRAIL}$.

9 Compare the average $T_{CLK\text{-}TRAIL}$ value with the conformance test limit.

Test References

See Table 14 - Global Operation Timing Parameters, in the *MIPI Alliance Standard for D-PHY v0.9*.

LP Exit: CLK Tx TEOT Test Method of Implementation

This test verifies the time from start of $T_{CLK\text{-}TRAIL}$ period to start of LP-11 state is within the conformance limit.

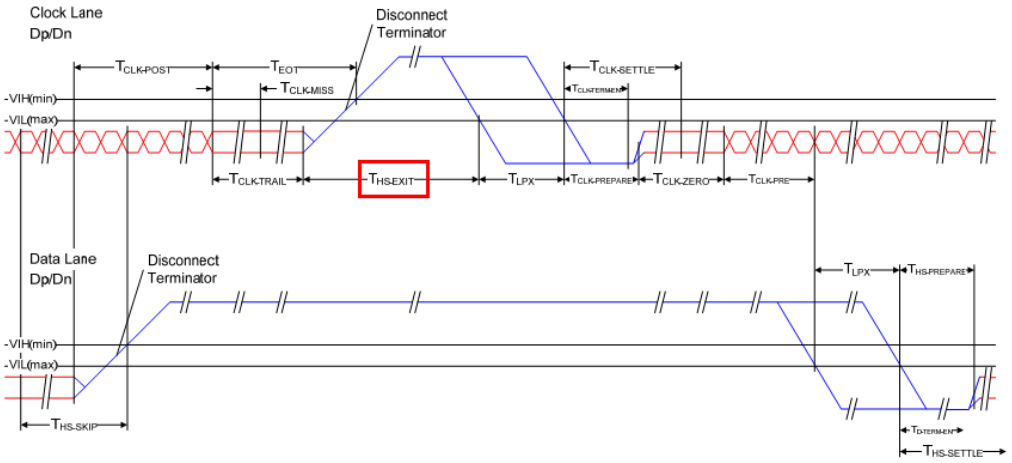

Figure 45 Switching the Clock Lane Between Clock Transmission and Low-Power Mode

Test Definition Notes from the Specification

Table 44 Global Operation Timing Parameters

Parameters	Description	Min	Typ	Max	Units	Notes
T_{EOT}	Time from start of $T_{HS\text{-}TRAIL}$ or $T_{CLK\text{-}TRAIL}$ period to start of LP-11 state			105 ns+n*12*UI	ns	3

NOTE 3: Where n = 1 for Forward-direction HS mode and n = 4 for Reverse-direction HS mode.

PASS Condition

The average T_{EOT} value must be equal or less than the conformance limit as specified in Table 14 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1 Trigger on the Clkn's falling edge after LP-01.

2 Back trace to the previous EoT.

3 Construct the differential clock waveform by using the following equation:

DiffClock = Clkp- Clkn

4 Find the time when the DiffClock crosses +/- V_{IDTH}(max) after last payload clock bit and denote it as T6.

5 Find the time when the Clkp Tx rising edge crosses V_{IH}(min). Denote the time as T8. Note that T8 must be greater than T6.

6 Calculate T_{EOT} by using the following equation:

T_{EOT} = T8- T6

7 Repeat step 1 to step 6 for a required number of observations.

8 Report the average T_{EOT}.

9 Compare the average T_{EOT} value with the conformance test limit.

Test References

See Table 14 - Global Operation Timing Parameters, in the *MIPI Alliance Standard for D-PHY v0.9*.

Part III
HS Data-Clock Timing

Agilent Technologies

8 High Speed (HS) Data-Clock Timing Tests

This section provides the Methods of Implementation (MOIs) for the High Speed (HS) Data-Clock Timing tests using an Agilent 80000, 90000, or 9000 Series Infiniium oscilloscope, differential probe amplifier, recommended probe heads and the MIPI D-PHY Conformance Test Application.

Probing for High Speed Data-Clock Timing Tests

When performing the HS Data-Clock Timing tests, the MIPI D-PHY Conformance Test Application will prompt you to make the proper connections. The connections for the HS Data-Clock Timing tests may look similar to the following diagram. Refer to the Connection tab in MIPI D-PHY Conformance Test application for the exact number of probe connections.

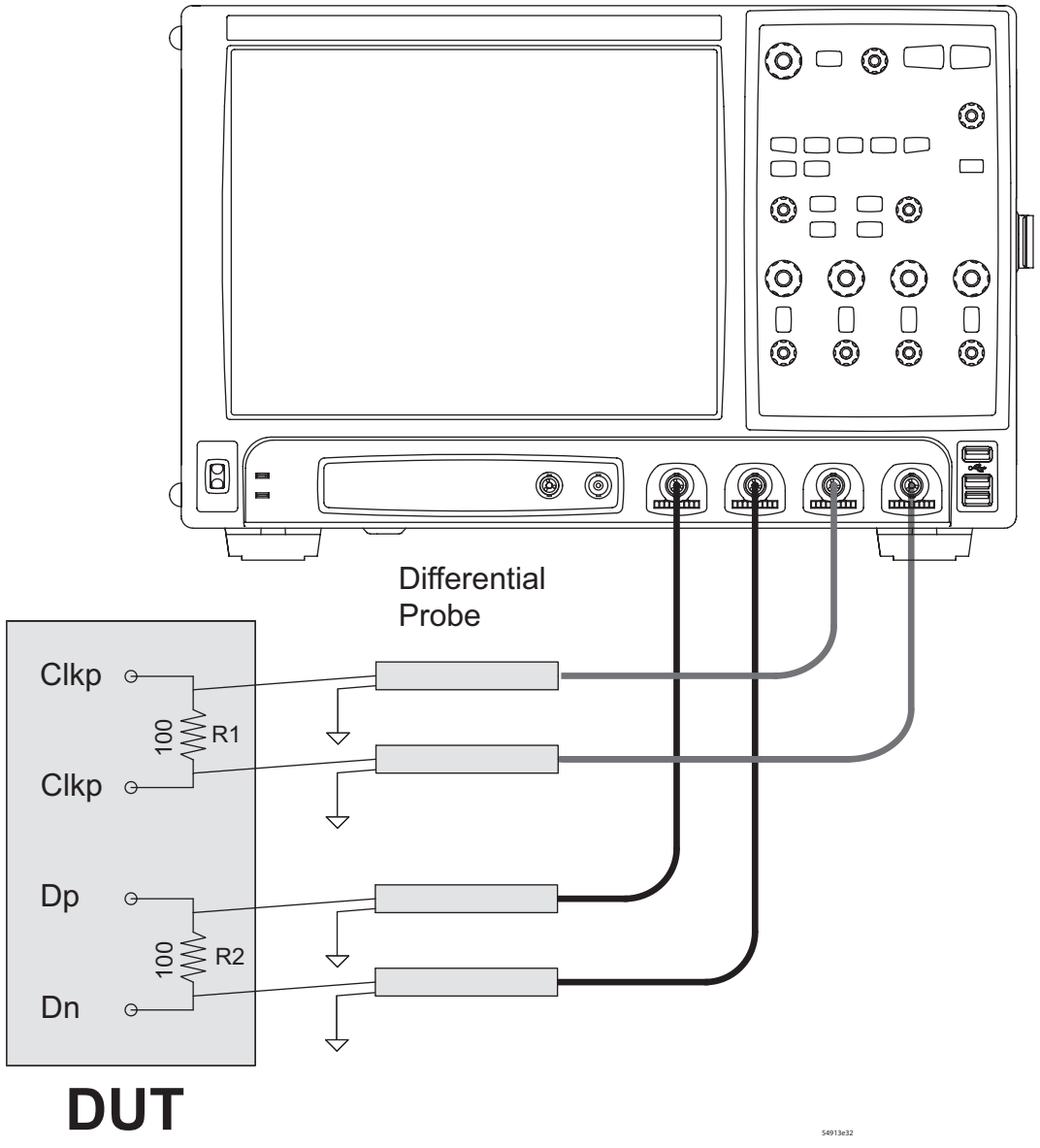

Figure 46 Probing for HS Data-Clock Timing Tests

You can identify the channels used for each signal in the Configuration tab of the MIPI D-PHY Conformance Test Application. (The channels shown in Figure 46 are just examples).

For more information on the probe amplifiers and probe heads, see Chapter 10, “InfiniiMax Probing,” starting on page 157.

Test Procedure

1 Start the automated test application as described in “Starting the MIPI D-PHY Conformance Test Application" on page 21.

2 In the MIPI D-PHY Conformance Test application, click the Set Up tab.

3 Enter the High-Speed Data Rate, Device ID and User Comments.

4 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

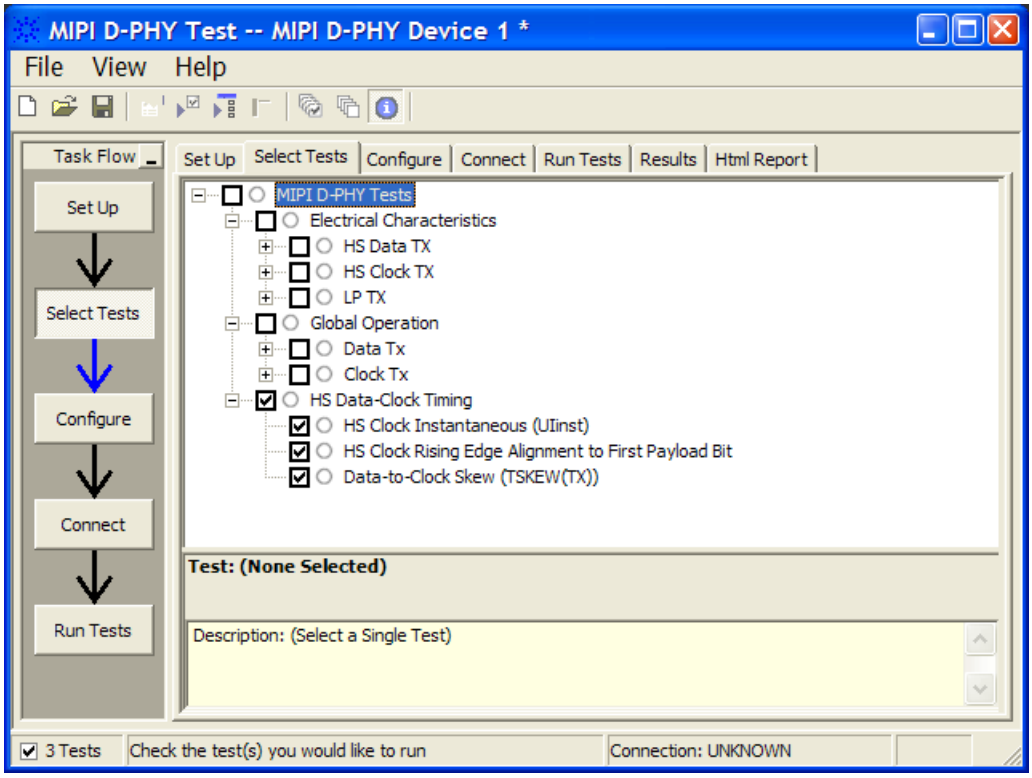

Figure 47 Selecting HS Data-Clock Timing Tests

5 Follow the MIPI D-PHY Conformance Test application’s task flow to set up the configuration options (see Table 45), run the tests and view the tests results.

Table 45 Test Configuration Options

Configuration Option	Description
Scope Channel Resources	
Dp	Identifies the oscilloscope channels probing Dp signal.
Dn	Identifies the oscilloscope channels probing Dn signal.
CLK(Diff)	Identifies the oscilloscope channels probing clock (differentially).
CLKp	Identifies the oscilloscope channels probing clock.
CLKn	Identifies the oscilloscope channels probing clock.

HS Clock Instantaneous Test Method of Implementation

This test verifies that the HS Clock transmitted by Clock Tx during HS Data burst does not exceed the required maximum value.

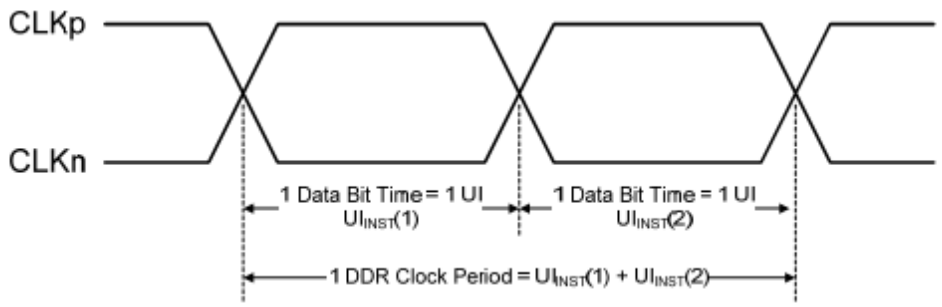

Figure 48 DDR Clock Definition

Test Definition Notes from the Specification

Table 46 Clock Signal Specification

Clock Parameter	Symbol	Min	Typ	Max	Units	Notes
UI instantaneous	UI_{INST}	150	200	12,5	ns	1,2

NOTE 1: This value corresponds to a minimum 80 Mbps data rate.

NOTE 2: The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

PASS Condition

The maximum Instantaneous UI must be within the conformance limit as specified in Table 26 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Ensure that the DUT's clock Tx does not go into LP mode during the test.
2. Capture Clkp and Clkn waveform.
3. Measure the min, max and average Unit Interval of the differential clock waveform.
4. Report the measurement min, max and average Unit Interval values.

5 Compare the maximum Unit Interval value with the conformance test limits.

Test References

See Table 26 - Clock Signal Specification, in the *MIPI Alliance Standard for D-PHY v0.9*.

HS Clock Rising Edge Alignment to First Payload Bit Test Method of Implementation

This test verifies that the first payload bit of the HS transmission burst aligns with differential HS clock's rising edge.

Test Definition Notes from the Specification

-

PASS Condition

The number of violation must be zero for the test to be considered as pass.

Measurement Algorithm

1. Trigger on Dn's falling edge after LP-01.
2. Find the first payload bit which is the first bit that comes after HS sync sequence.
3. Construct the differential clock waveform by using the following equation:

   DiffClock = Clkp-Clkn
4. Ensure that in the first payload bit, there is a DiffClock rising edge during the bit period.
5. Repeat step 1 to 5 for a number of required observations.
6. Record the number of violation.
7. Compare the number of violations and make sure that none of them is greater than 0.

Test References

-

Data-to-CLock Skew (TSKEW(Tx)) Test Method of Implementation

This test verifies that the Data to Clock Skew, measured at transmitter is within the required specification.

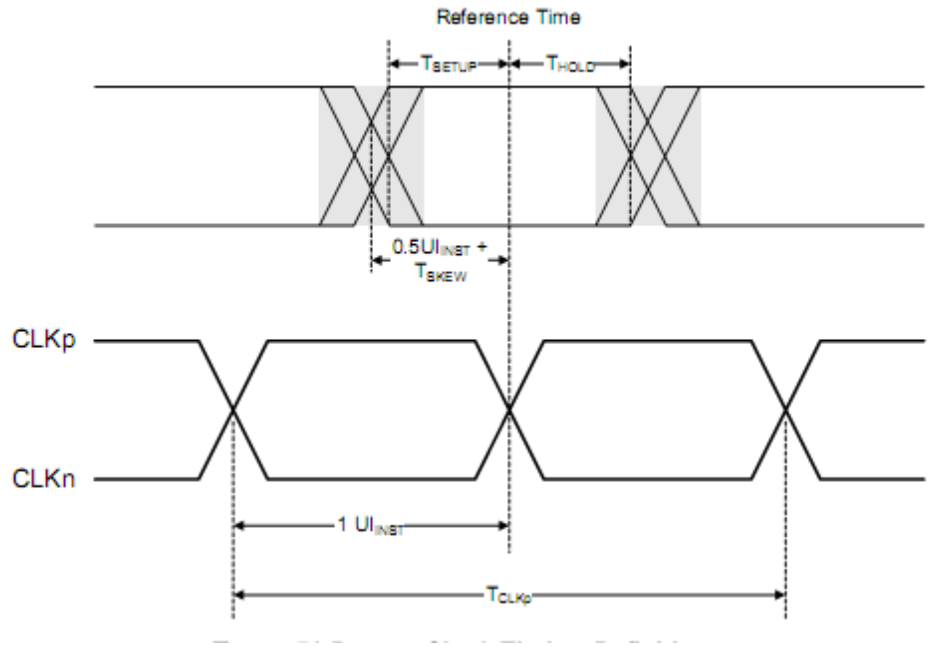

Figure 49 Data to Clock Timing Definitions

Test Definition Notes from the Specification

Table 47 Data-Clock Timing Specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
Data to Clock Skew (measured at transmitter)	$T_{SKEW(TX)}$	-0.15		0.15	UI_{INST}	1

NOTE 1: Total silicon and package delay budget of $0.3*UI_{INST}$.

PASS Condition

The $T_{SKEW(TX)}$ in UI must be within the conformance limit as specified in Table 27 of the MIPI Alliance Standard for D-PHY document.

Measurement Algorithm

1. Dp, Dn, Clkp and Clkn waveforms are captured during the HS burst.
2. Construct the differential clock waveform by using the following equation:

   DiffClock = Clkp-Clkn
3. Construct the differential data waveform by using the following equation:

   DiffData = Dp-Dn
4. By using the DiffClock's rising and falling edges, fold the DiffData to form a data eye.
5. Find the min of the histogram, which is the time when the left most edge crosses the DiffData crossing level.
6. Calculate $T_{SKEW(TX)}$ in seconds and UI by using the following equation:

   $T_{SKEW(TX)}$ (in seconds) = (TLeftMostEdge-TCenter)-0.5*MeanUI

   $T_{SKEW(TX)}$ (in UI) = $T_{SKEW(TX)}$/MeanUI
7. Report the $T_{SKEW(TX)}$ in seconds and in UI.
8. Compare the $T_{SKEW(TX)}$ value with the conformance test limits.

Test References

See Table 27 - Data-Clock Timing Specifications, in the *MIPI Alliance Standard for D-PHY v0.9*.

Part IV
Appendices

Agilent Technologies

9 Calibrating the Infiniium Oscilloscopes and Probes

This section describes the Agilent Infiniium oscilloscopes calibration procedures.

To Run the Self Calibration

NOTE Let the Oscilloscope Warm Up Before Adjusting. Warm up the oscilloscope for 30 minutes before starting calibration procedure. Failure to allow warm up may result in inaccurate calibration.

The self calibration uses signals generated in the oscilloscope to calibrate channel sensitivity, offsets, and trigger parameters. You should run the self calibration

- yearly, or according to your periodic needs,
- when you replace the acquisition assembly or acquisition hybrids,
- when you replace the hard drive or any other assembly,
- when the oscilloscope's operating temperature (after the 30 minute warm-up period) is more than ±5 °C different from that of the last calibration.

To calibrate the 90000 Series Infiniium oscilloscope in preparation for running the MIPI D-PHY automated tests, you need the following equipment:

Table 48 Equipment Required

Equipment	Critical Specifications	Agilent Part Number
Adapters (2 supplied with oscilloscope except for the DSO90254A)	3.5 mm (f) to precision BNC No substitute	Agilent 54855-67604
Cable Assembly	50 Ù characteristic impedance BNC (m) connectors ~ 36 inches (91 cm) to 48 inches (122 cm) long	Agilent 8120-1840
Cable Assembly (supplied with oscilloscope except for the DSO90254A which can use a good quality BNC cable)	No substitute	Agilent 54855-61620
10 MHz Signal Source (required for time scale calibration)	Frequency accuracy better than 0.4 ppm	Agilent 53131A with Opt. 010

Self Calibration

NOTE Calibration time: It will take approximately 1 hour to run the self calibration on the oscilloscope, including the time required to change cables from channel to channel.

1 Let the Oscilloscope Warm Up Before Running the Self Calibration.

The self calibration should only be done after the oscilloscope has run for 30 minutes at ambient temperature with the cover installed. Calibration of an oscilloscope that has not warmed up may result in an inaccurate calibration.

2 Pull down the Utilities menu and Select Calibration.

3 Click the check box to clear the Cal Memory Protect condition.

You cannot run self calibration if this box is checked. See Figure 50.

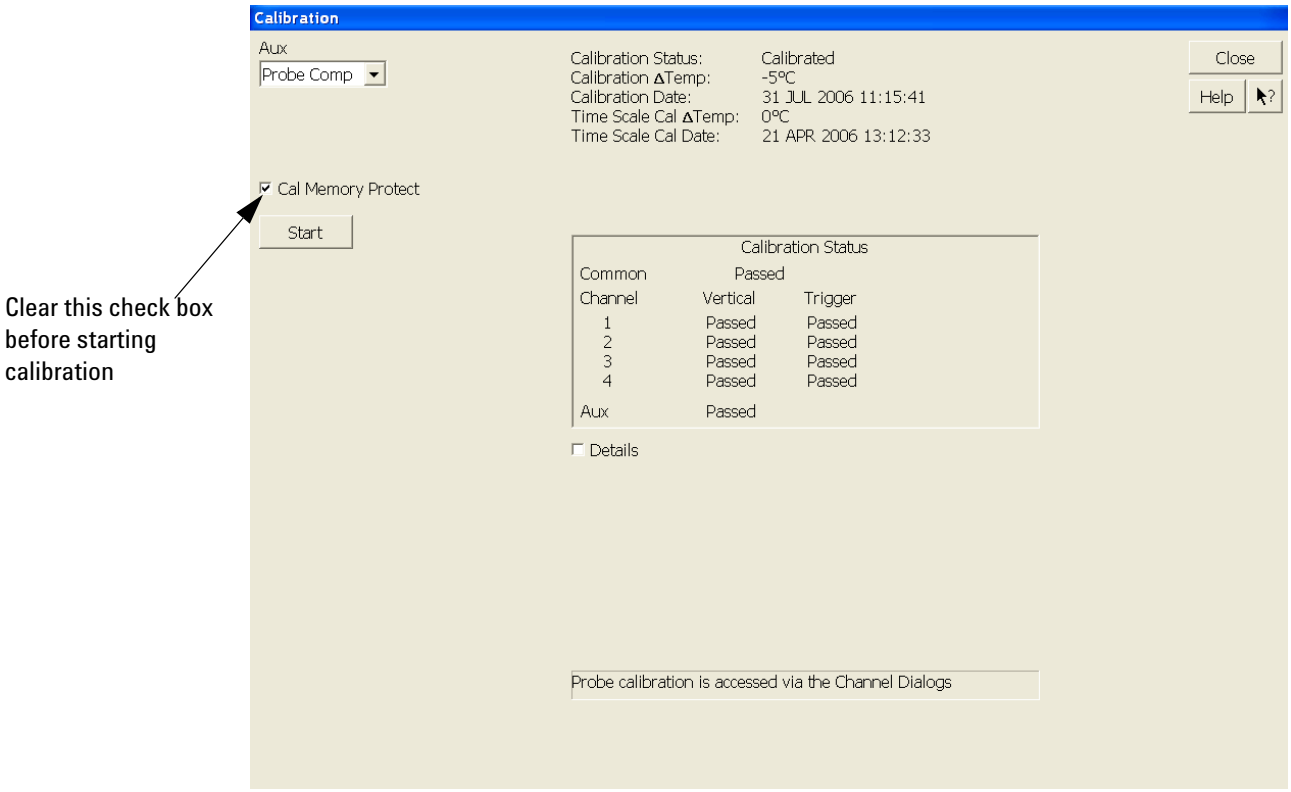

Figure 50 Oscilloscope Calibration Window

4 Click Start, then follow the instructions on the screen.

The routine will ask you to do the following things in sequence:

a Decide if you want to perform the Time Scale Calibration. Your choices are:

- Standard Calibration - Time scale calibration will not be performed. Time scale calibration factors from the previous time scale calibration will be used and the 10 MHz reference signal will not be required. The remaining calibration procedure will continue.
- Standard Calibration and Time Scale Calibration - Performs the time scale calibration. This option requires you to connect a 10 MHz reference signal to channel 1 that meets the following specifications. Failure to use a reference signal that meets this specification will result in an inaccurate calibration.

  Frequency: 10 MHz ±0.4 ppm = 10 MHz ±4 Hz

  Amplitude: 0.2 Vpeak-to-peak to 5.0 Vpeak-to-peak

  Wave shape: Sine or Square

- Standard Calibration and Reset Time Scale Calibration - Factory time scale calibration factors will be used. The 10 MHz reference signal will not be required. The remaining calibration procedure will continue.

b Disconnect everything from all inputs and Aux Out.

c Connect the calibration cable from Aux Out to channel 1.

- You must use the 54855-61620 cable assembly with two 54855-67604 adapters for all oscilloscopes except for the DSO90254A which can use a good quality BNC cable. Failure to use the appropriate calibration cable will result in an inaccurate calibration.

d Connect the calibration cable from Aux Out to each of the channel inputs as requested.

e Connect the 50 Ù BNC cable from the Aux Out to the Aux Trig on the front panel of the oscilloscope.

f A Passed/Failed indication is displayed for each calibration section. If any section fails, check the calibration cables and run the oscilloscope Self Test in the Utilities menu.

g Once the calibration procedure is completed, click Close.

Required Equipment for Solder-in and Socketed Probe Heads Calibration

NOTE Each probe is calibrated with the oscilloscope channel to which it is connected. Do not switch probes between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the probes be labeled with the channel on which they were calibrated.

Before performing MIPI D-PHY tests you should calibrate the probes. Calibration of the solder-in probe heads consist of a vertical calibration and a skew calibration. The vertical calibration should be performed before the skew calibration. Both calibrations should be performed for best probe measurement performance.

The calibration procedure requires the following parts.

- BNC (male) to SMA (male) adaptor
- Deskew fixture
- 50 Ω SMA terminator

Calibration for Solder-in and Socketed Probe Heads

NOTE Before calibrating the probe, verify that the Infiniium oscilloscope has been calibrated recently and that the calibration temperature is within ±5 °C. If this is not the case, calibrate the oscilloscope before calibrating the probe. This information is found in the Infiniium Calibration dialog box.

Connecting the Probe for Calibration

For the following procedure, refer to Figure 51 below.

1. Connect BNC (male) to SMA (male) adaptor to the deskew fixture on the connector closest to the yellow pincher.
2. Connect the 50 Ω SMA terminator to the connector farthest from yellow pincher.
3. Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.
4. Connect the probe to an oscilloscope channel.
5. To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.
6. Push down the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.
7. Release the yellow pincher.

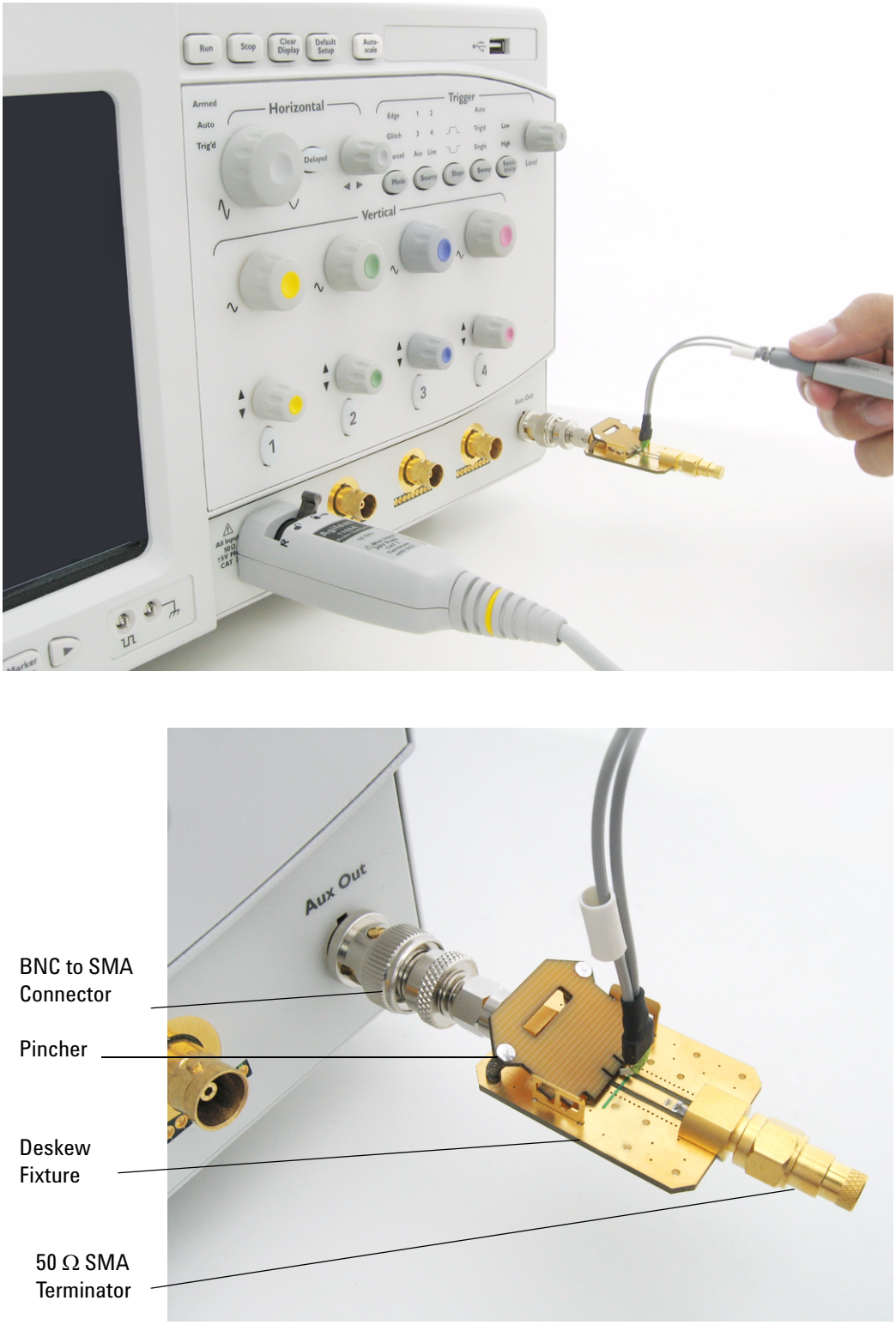

Figure 51 Solder-in Probe Head Calibration Connection Example

Verifying the Connection

1 On the Infiniium oscilloscope, press the autoscale button on the front panel.

2 Set the volts per division to 100 mV/div.

3 Set the horizontal scale to 1.00 ns/div.

4 Set the horizontal position to approximately 3 ns. You should see a waveform similar to that in Figure 52 below.

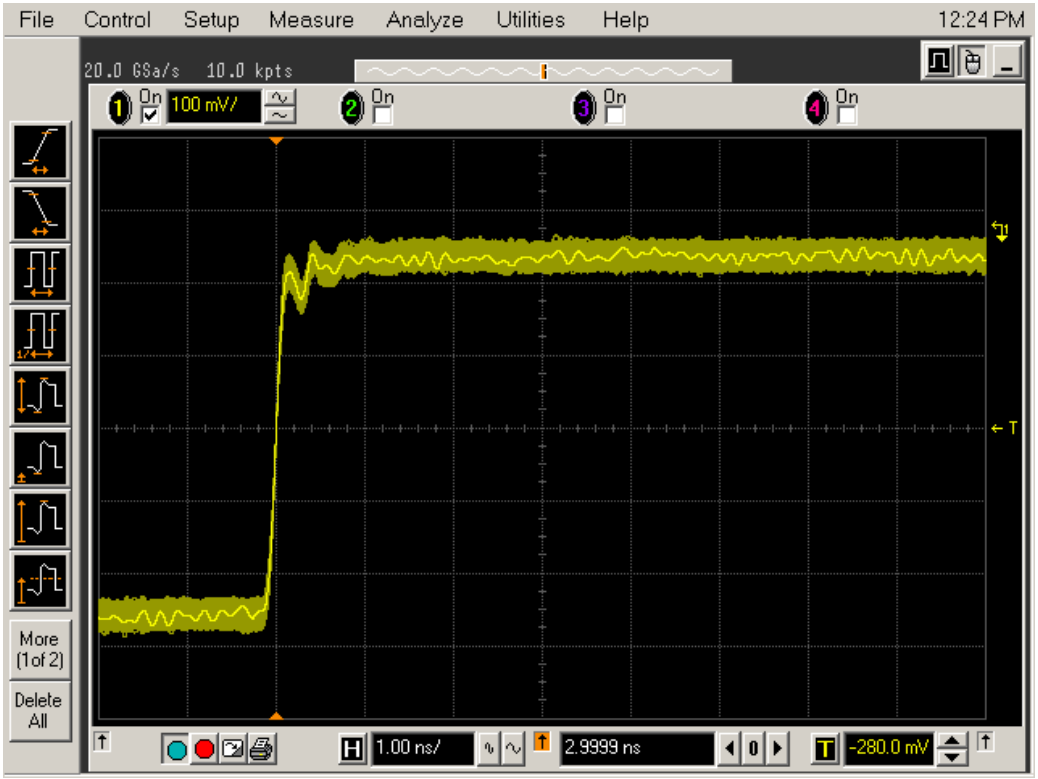

Figure 52 Good Connection Waveform Example

If you see a waveform similar to that of Figure 53 below, then you have a bad connection and should check all of your probe connections.

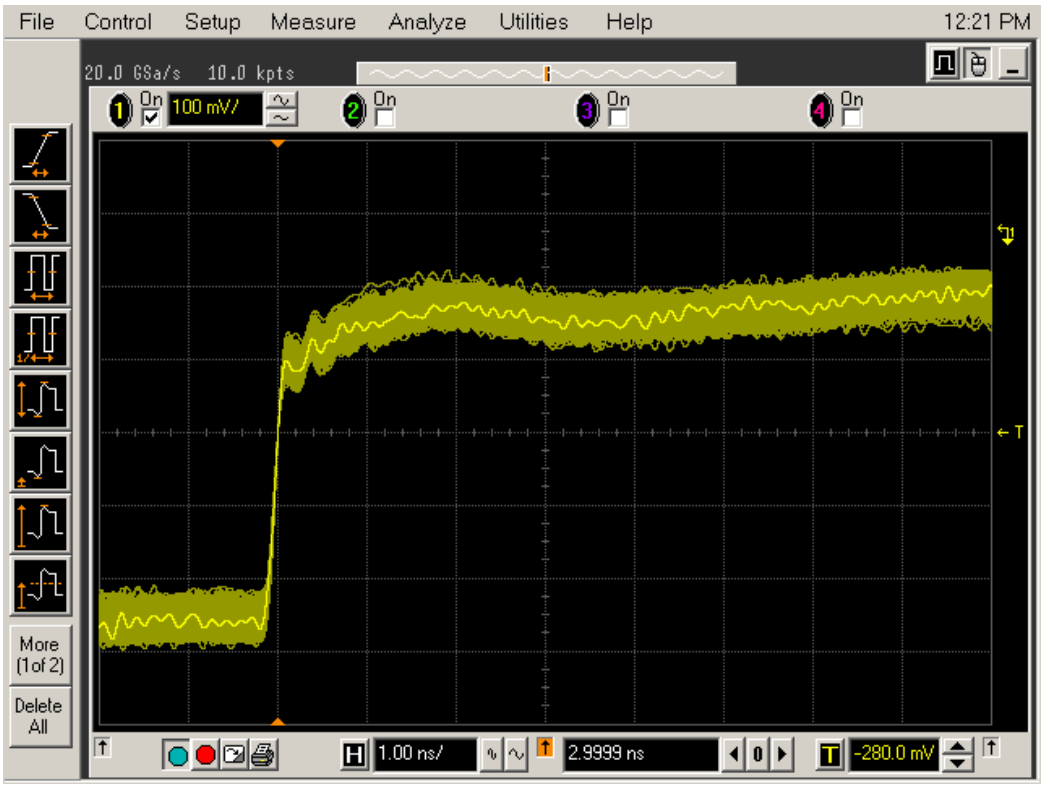

Figure 53 Bad Connection Waveform Example

Running the Probe Calibration and Deskew

1 On the Infiniium oscilloscope in the Setup menu, select the channel connected to the probe, as shown in Figure 54.

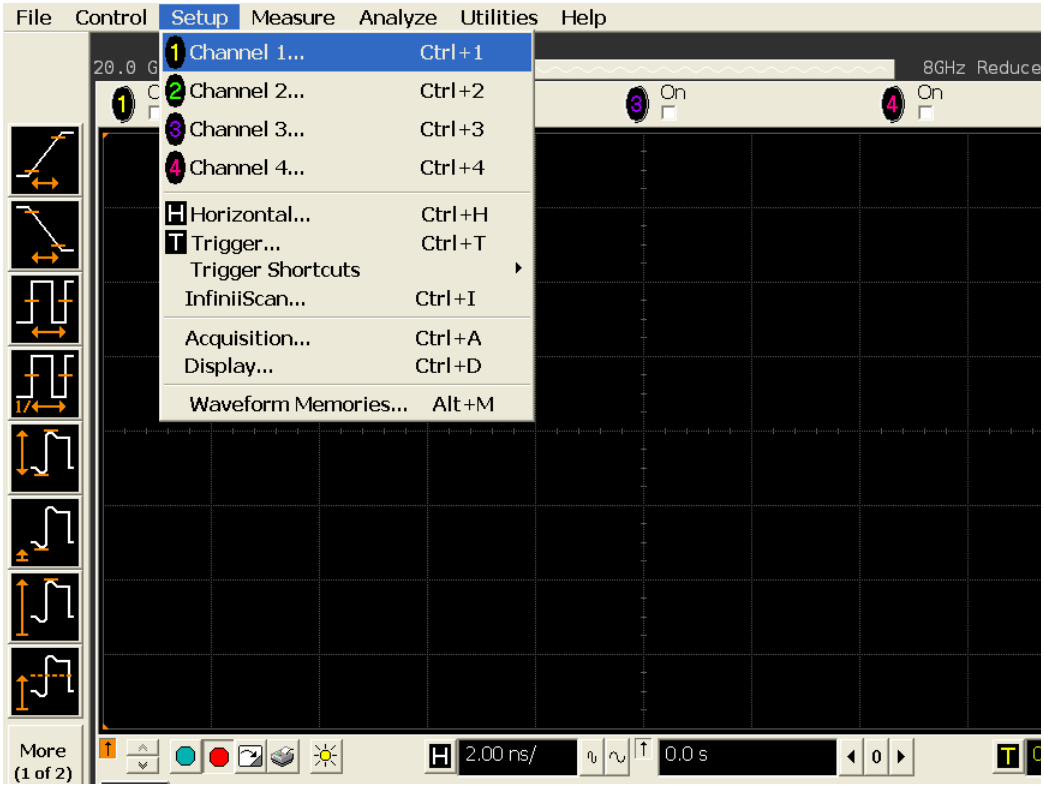

Figure 54 Channel Setup Window.

2 In the Channel Setup dialog box, select the Probes... button, as shown in Figure 55.

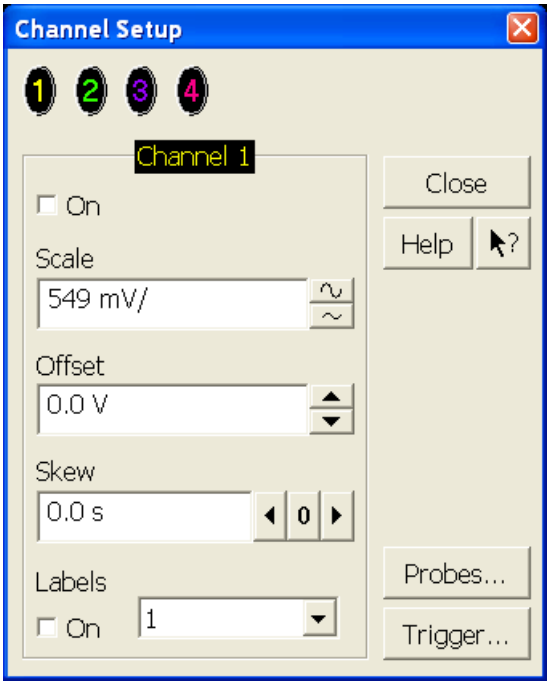

Figure 55 Channel Dialog Box

3 In the Probe Setup dialog box, select the Calibrate Probe... button.

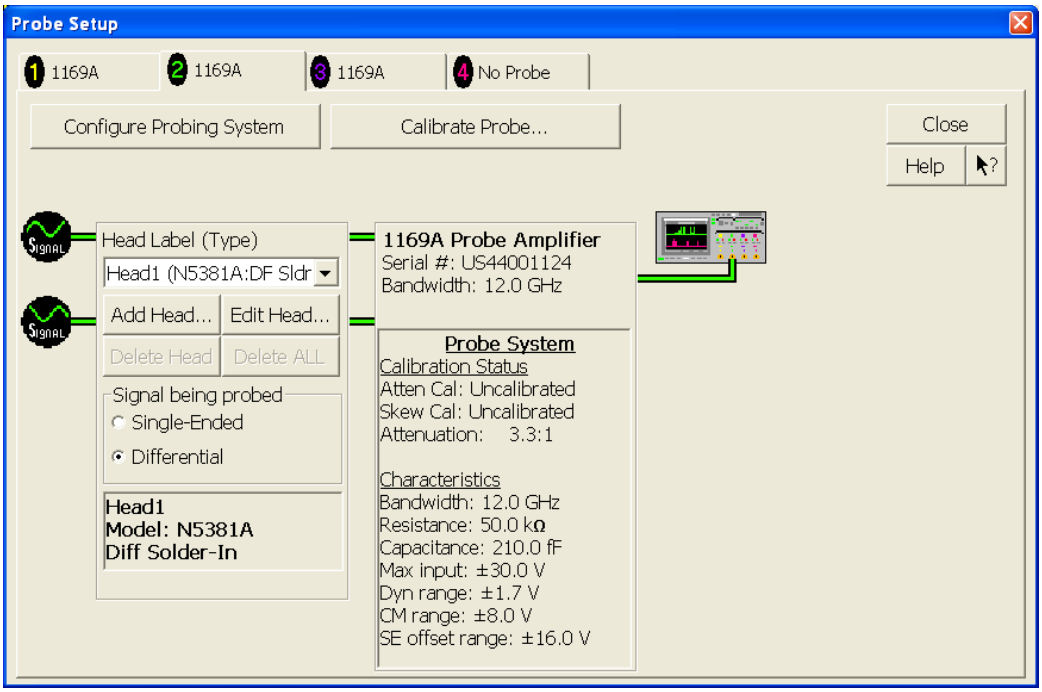

Figure 56 Probe Setup Window.

4 In the Probe Calibration dialog box, select the Calibrated Atten/Offset radio button.

5 Select the Start Atten/Offset Calibration... button and follow the on-screen instructions for the vertical calibration procedure.

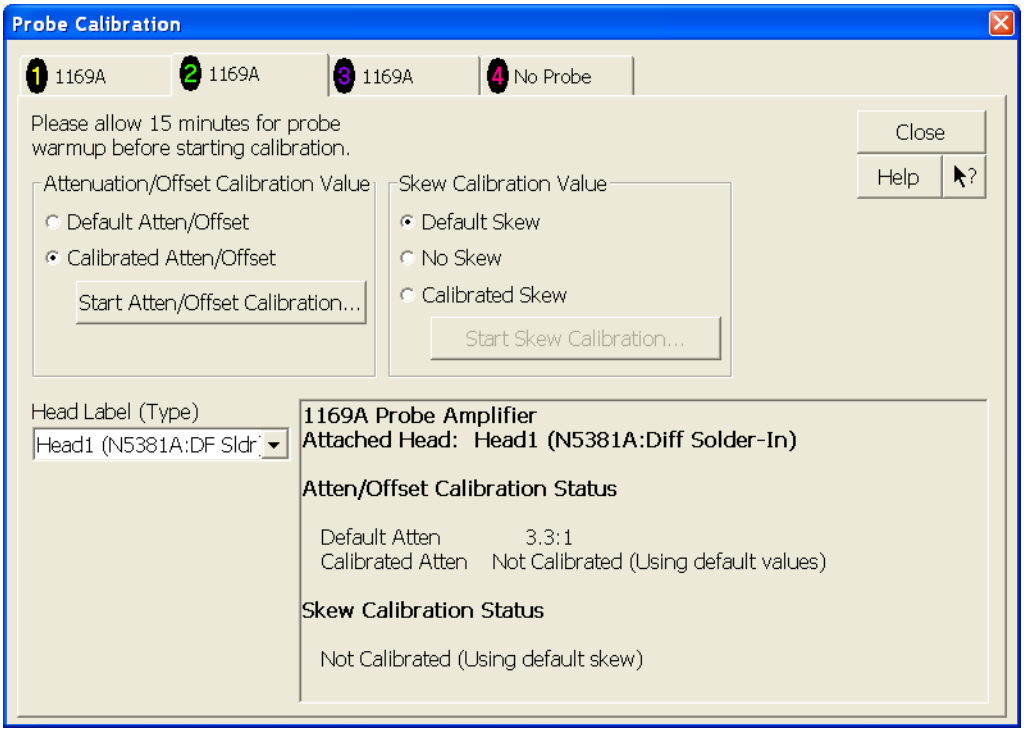

Figure 57 Probe Calibration Window.

6 Once the vertical calibration has successfully completed, select the Calibrated Skew... button.

7 Select the Start Skew Calibration... button and follow the on-screen instructions for the skew calibration.

At the end of each calibration, the oscilloscope will prompt you if the calibration was or was not successful.

Verifying the Probe Calibration

If you have successfully calibrated the probe, it is not necessary to perform this verification. However, if you want to verify that the probe was properly calibrated, the following procedure will help you verify the calibration.

The calibration procedure requires the following parts:

- BNC (male) to SMA (male) adaptor
- SMA (male) to BNC (female) adaptor
- BNC (male) to BNC (male) 12 inch cable such as the Agilent 8120-1838
- Agilent 54855-61620 calibration cable (Infiniium oscilloscopes with bandwidths of 6 Ghz and greater only)
- Agilent 54855-67604 precision 3.5 mm adaptors (Infiniium oscilloscopes with bandwidths of 6 Ghz and greater only)
- Deskew fixture

For the following procedure, refer to Figure 58.

1 Connect BNC (male) to SMA (male) adaptor to the deskew fixture on the connector closest to the yellow pincher.

2 Connect the SMA (male) to BNC (female) to the connector farthest from the yellow pincher.

3 Connect the BNC (male) to BNC (male) cable to the BNC connector on the deskew fixture to one of the unused oscilloscope channels. For infiniium oscilloscopes with bandwidths of 6 GHz and greater, use the 54855-61620 calibration cable and the two 54855-64604 precision 3.5 mm adaptors.

4 Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.

5 Connect the probe to an oscilloscope channel.

6 To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.

7 Push down on the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.

8 Release the yellow pincher.

9 On the oscilloscope, press the autoscale button on the front panel.

10 Select Setup menu and choose the channel connected to the BNC cable from the pull-down menu.

11 Select the Probes... button.

12 Select the Configure Probe System button.

13 Select User Defined Probe from the pull-down menu.

14 Select the Calibrate Probe... button.

15 Select the Calibrated Skew radio button.

16 Once the skew calibration is completed, close all dialog boxes.

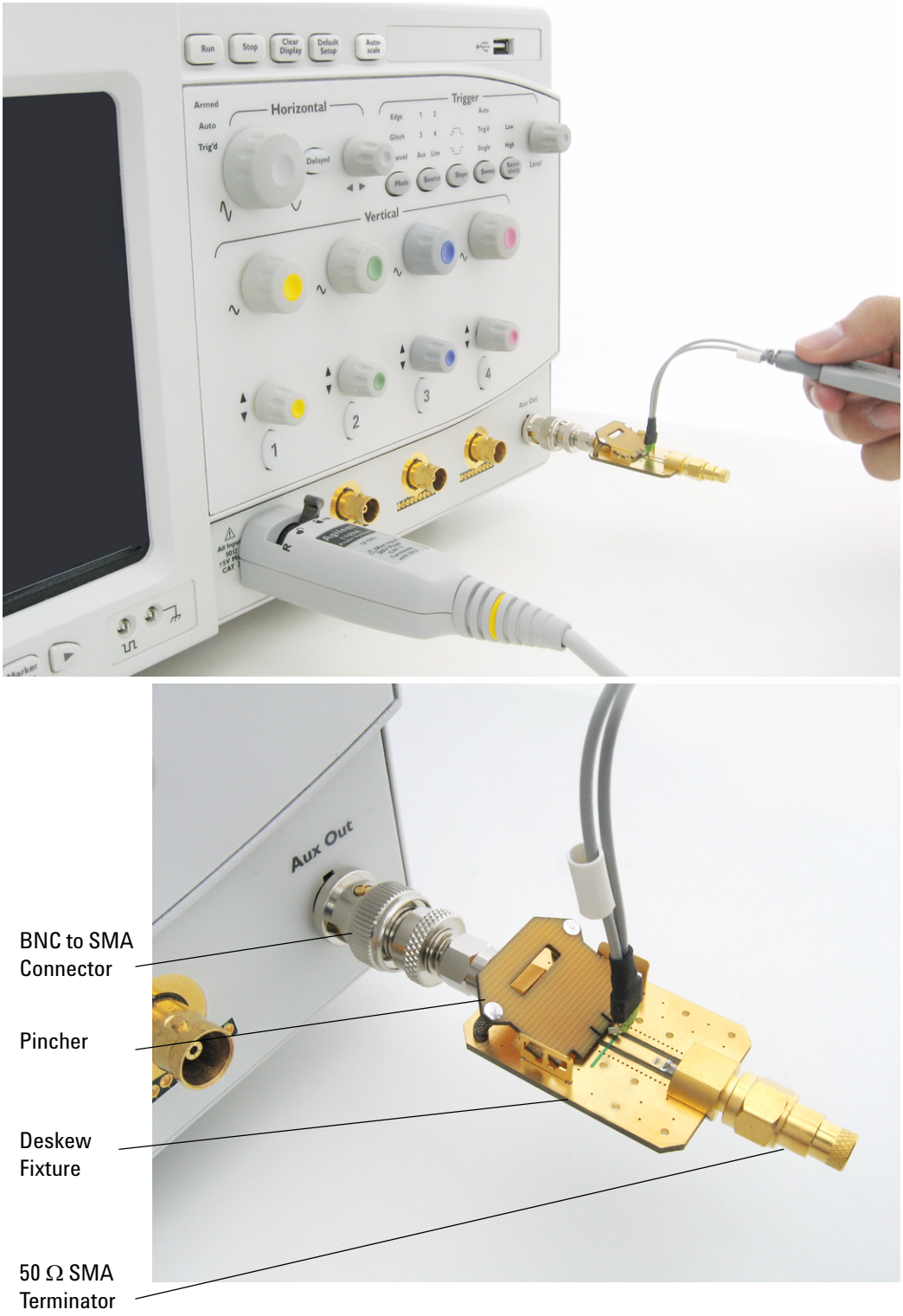

Figure 58 Probe Calibration Verification Connection Example

17 Select the Start Skew Calibration... button and follow the on-screen instructions.

18 Set the vertical scale for the displayed channels to 100 mV/div.

19 Set the horizontal range to 1.00 ns/div.

20 Set the horizontal position to approximately 3 ns.

21 Change the vertical position knobs of both channels until the waveforms overlap each other.

22 Select the Setup menu and choose Acquisition... from the pull-down menu.

23 In the Acquisition Setup dialog box enable averaging. When you close the dialog box, you should see waveforms similar to that in Figure 59.

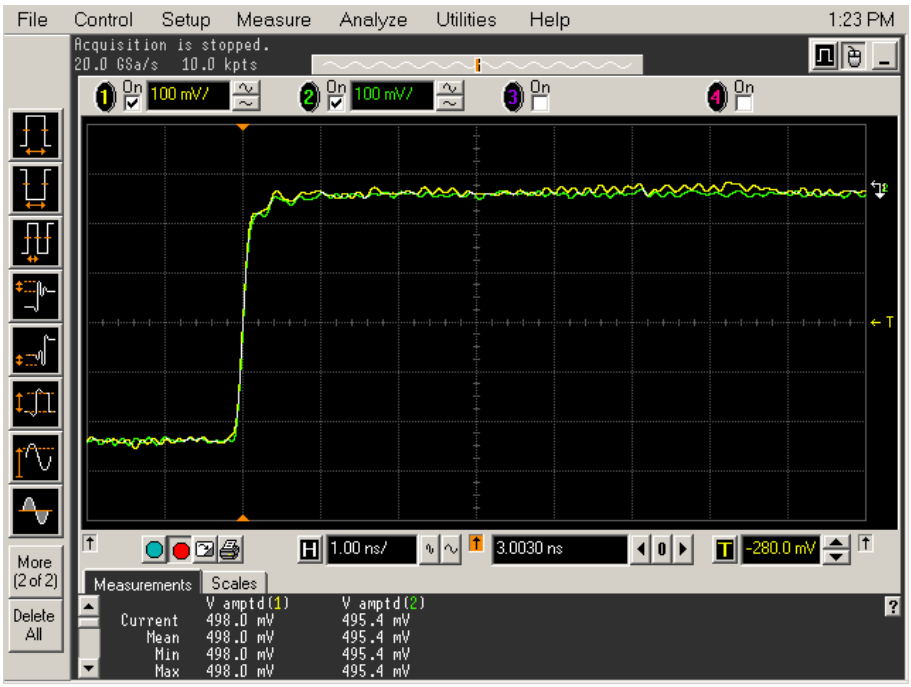

Figure 59 Calibration Probe Waveform Example

Required Equipment for Browser Probe Head Calibration

NOTE Before calibrating the probe, verify that the Infiniium oscilloscope has been calibrated recently and that the calibration temperature is within ±5 °C. If this is not the case, calibrate the oscilloscope before calibrating the probe. This information is found in Infiniium Calibration dialog box.

Calibration of the hand-held browser probe heads consists of a vertical calibration and a skew calibration. The vertical calibration should be performed before the skew calibration. Both calibrations should be performed for the best probe measurement performance.

The calibration procedure requires the following parts.

- BNC (male) to SMA (male) adaptor
- Deskew fixture
- 50 Ω SMA terminator

Calibration for Browser Probe Head

Connecting the Probe for Calibration

For the following procedure, refer to Figure 60 below.

1. Connect BNC (male) to SMA (male) adaptor to the deskew fixture on the connector closest to the yellow pincher.
2. Connect the 50 Ω SMA terminator to the connector farthest from the yellow pincher.
3. Connect the BNC side of the deskew fixture to the Aux Out of the Infiniium oscilloscope.
4. Connect the probe to an oscilloscope channel.
5. Place the positive resistor tip of the browser on the center conductor of the deskew fixture between the green line and front end of the yellow pincher. The negative resistor tip or ground pin of the browser must be on either of the two outer conductors (ground) of the deskew fixture.
6. On the Infiniium oscilloscope in the Setup menu, select the channel connected to the probe.
7. In the Channel Setup dialog box select the Probes... button.
8. In the Probe Setup dialog box select the Calibrate Probe... button.
9. In the Probe Cal dialog box select the Calibrated Atten/Offset radio button.
10. Select the Start Atten/Offset Calibration... button and follow the on-screen instructions for the vertical calibration procedure.

11 Once the vertical calibration has successfully completed, select the Calibrated Skew... button.

12 Select the Start Skew Calibration... button and follow the on-screen instructions for the skew calibration.

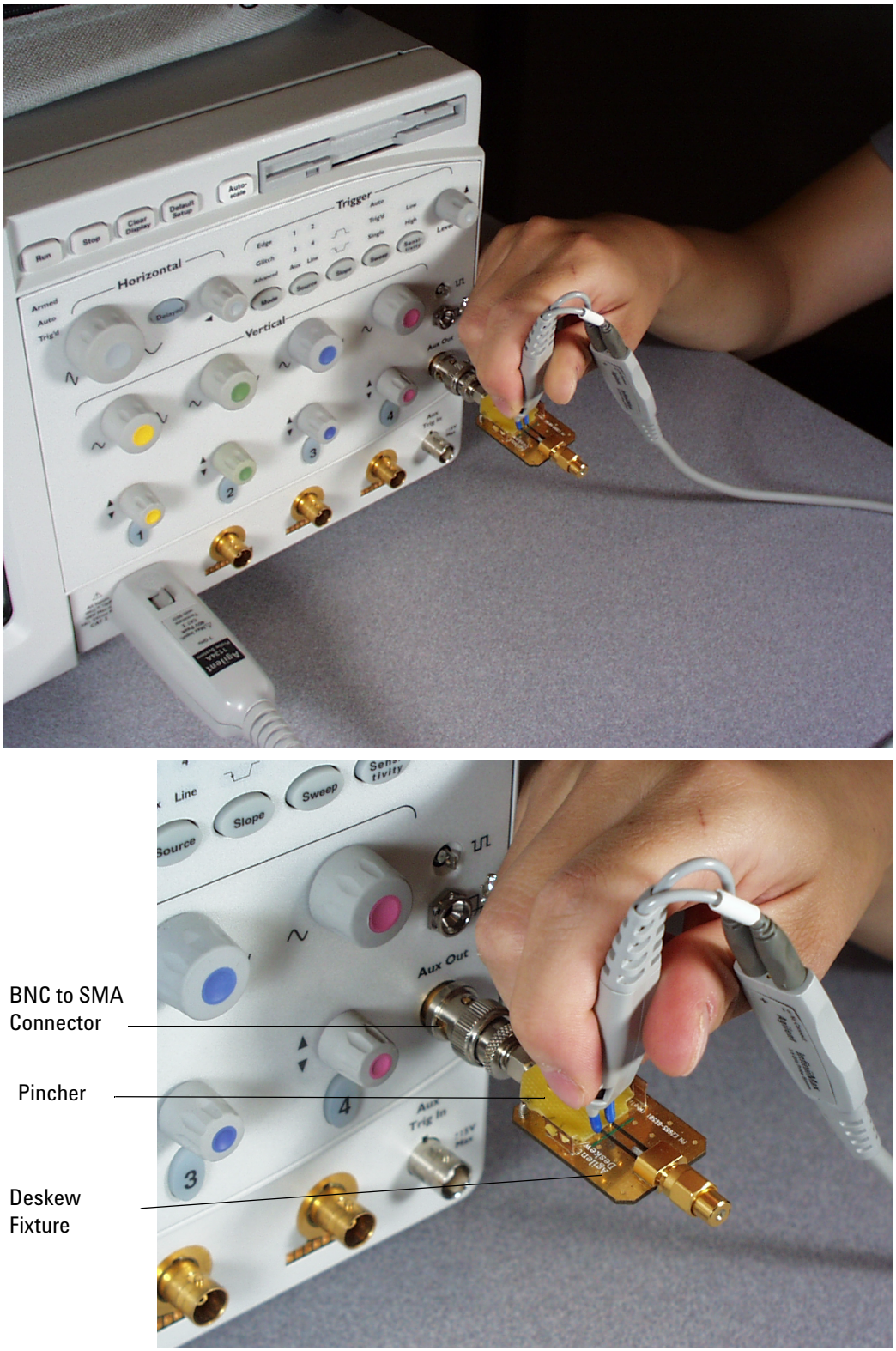

Figure 60 Browser Probe Head Calibration Connection Example

10 InfiniiMax Probing

Figure 61 1168A and 1169A InfiniiMax Probe Amplifier

Differential probe amplifier, with minimum bandwidth of 5 GHz is required.

Agilent recommends 1132A, 1134A, 1168A and 1169A probe amplifiers.

Table 49 Recommended InfiniiMax I and InfiniiMax II Series Probe Amplifiers

Model	Bandwidth	Description
1132A	5 GHz	InfiniiMax I probe amplifier
1134A	7 GHz	InfiniiMax I probe amplifier
1168A	10 GHz	InfiniiMax II probe amplifier
1169A	12 GHz	InfiniiMax II probe amplifier

Agilent also recommends E2677A differential solder-in probe head, E2675A differential browser probe head, E2678A differential socket probe head and E2669A differential kit which includes E2675A, E2677A and E2678A.

Figure 62 E2677A Differential Solder-in Probe Head

Table 50 Probe Head Characteristics (with 11684A and 1169A probe amplifiers with limitations)

Probe Head	Model Number	Differential Measurement (BW, input C, input R)	Single-Ended Measurement (BW, input C, input R)
Differential solder-in (Higher loading, high frequency response variation)	E2677A	12 GHz, 0.27 pF, 50 kOhm	12 GHz, 0.44 pF, 25 kOhm
Differential socket (Higher loading)	E2678A	12 GHz, 0.34 pF, 50 kOhm	7 GHz, 0.56 pF, 25 kOhm
Differential browser - wide span	E2675A	6 GHz, 0.32 pF, 50 kOhm	6 GHz, 0.57 pF, 25 kOhm
Differential kit	E2669A (includes E2675A, E2677A and E2678A)		

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